GaN Power HEMT Tutorial:
GaN Basics

GANPOWER INTERNATIONAL INC

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- Session 1: GaN devices basics
  - GaN, An Introduction
  - GaN Design, Fabrication and Testing
  - GaN Compact Modeling and Reliability
- Session 2: Gate Driving
- Session 3: GaN Applications

Power Devices: History of Evolvements

1952	1957	1960s	1970s	1980s	2000	2010
Power Diode Germanium	Thyristor Silicon	Power Bipolar Silicon	Power MOSFET Silicon	IGBT Silicon	Schottky diode Silicon Carbide	Power HEMT GaN

It's time to move on…

FOM

Figure of Merit (FOM)

Bipolar

VFET

HEXFET

TrenchFET

Super Junction

Next Gen Si

Silicon Maturation

GaN / SiC
Power Devices

Si

WBG

polysilicon gate
source contact
n-drift
region
n+
source
p+ body
contact
drain
n+
substrate
p-well

GaN vs Si
Power Consumption [mW]
600
500
400
300
200
100
0
Drive Power
Conduction loss
Switching loss
GaN
Si

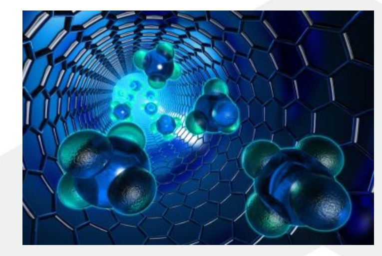
1978

2003

2009

Year

Material Properties Comparison



Material Property	Silicon	SiC-4H	GaN
Band-gap (eV)	1.1	3.2	3.4
Critical Field (1E+6V/cm)	0.3	3	3.5
Electron Mobility (cm^2/V-Sec.)	1450	900	2000
Electron Saturation Velocity (1E+6 cm/Sec.)	10	22	25
Thermal Conductivity (W/cm^2K)	1.5	3.8	1.3
Baliga Figure of Merit (FOM)=$\varepsilon_s \mu E_c^3$	1	675	3000

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WBG Power Devices: Applications

GaN HEMT → Encroaching → Silicon Super Junction MOSFET

SiC MOSFET → Encroaching → Silicon IGBT

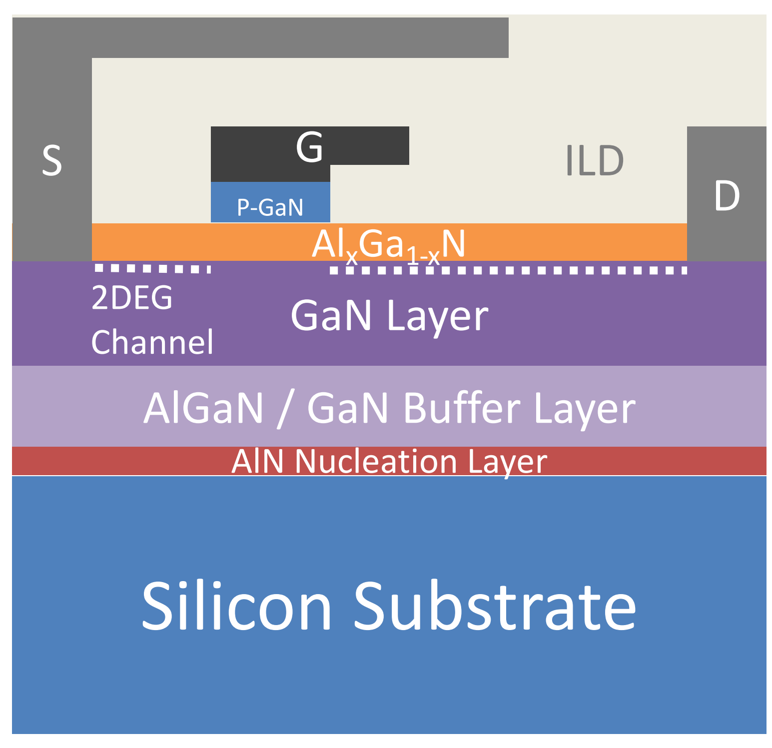
Source: Yole Development: How power electronics will reshape to meet 21st century challenges? ISPSD 2015

Substrate Materials for GaN HEMT

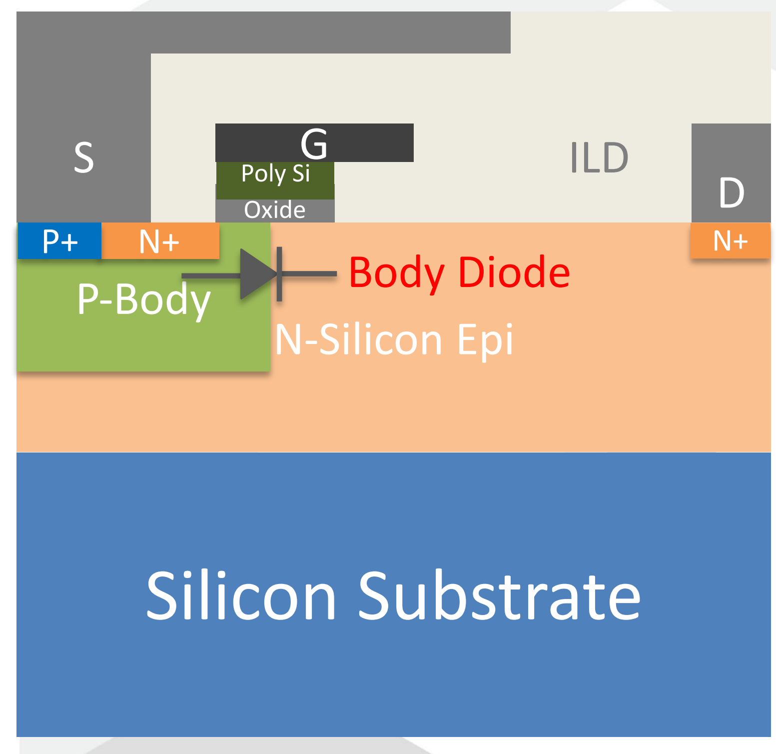
Attributes	Si sub.	SiC sub.	Sapphire	GaN sub
Defect density (cm^{-2})	1E+9	5E+8	3E+8	1E+3 to 1E+5
Lattice mismatch (%)	17	3.5	-16	0
Thermal conductivity (W/cm-k at 25 °C)	1.5	4.9	0.25	1.3
Coefficients of thermal expansions (%)	54	25	34	0
Off-state leakage	high	high	low	low
Reliability and yield	low	low	low	high
Lateral or Vertical device	lateral	lateral	lateral	lateral or vertical
Integration possibility	Very high	Moderate	Moderate	-
Substrate size (mm)	300	150	100	50
Substrate cost (relative)	Low	high	Low	Very high

Power RF

Simplified E-GaN vs. LDMOS Device Structures



GaN HEMT



Silicon LDMOS

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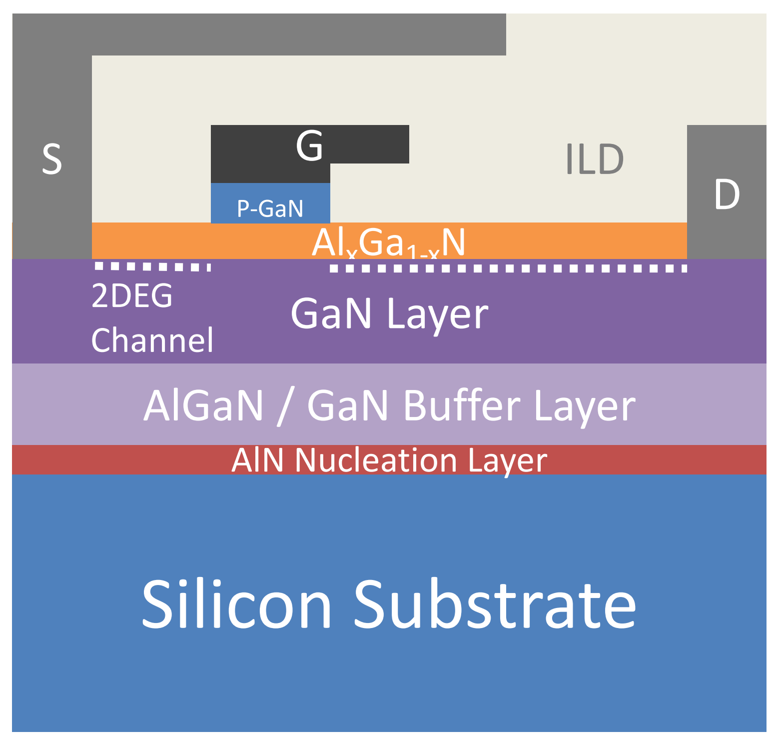
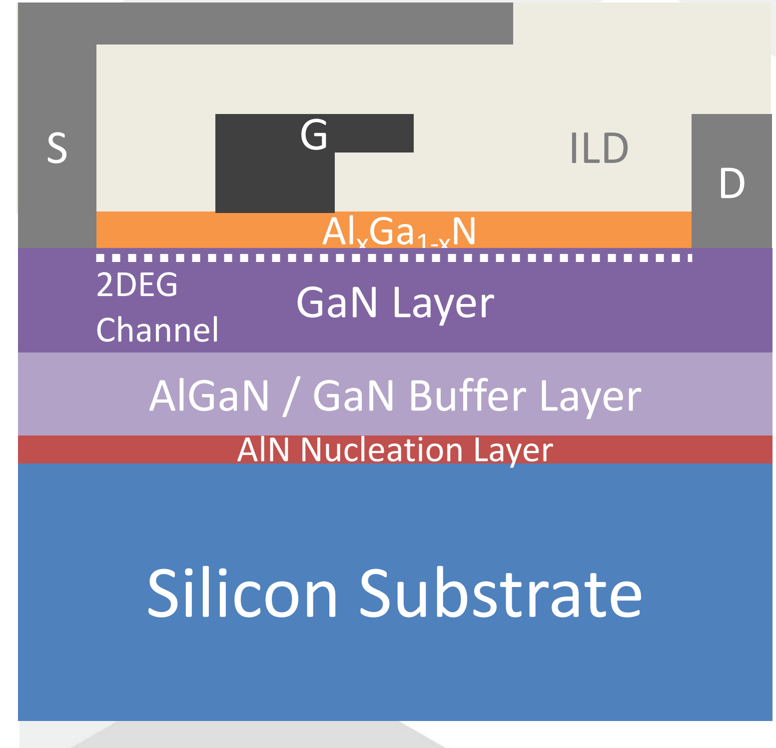
Simplified E-Mode vs. D-Mode GaN HEMT



E-Mode GaN HEMT



D-Mode GaN HEMT

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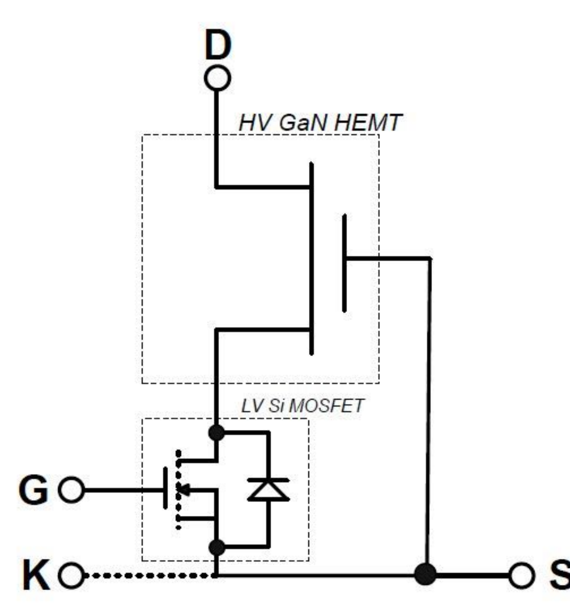
Cascode GaN HEMT



Good:

- GaN is normally on by nature: easy to fabricate
- Si like gate control with higher V_{th}
- Reverse conduction with LV MOS body-diode

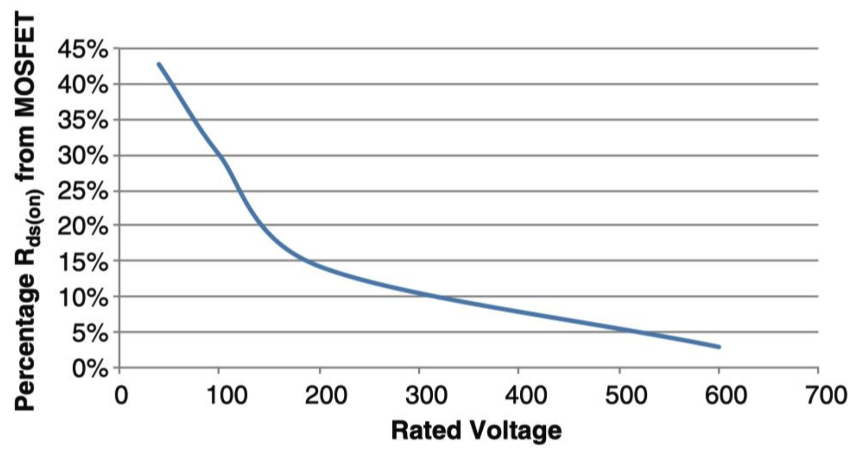
Bad:

- Comparatively lower performance
- Controlling silicon rather than GaN gate
- May need extra TVS device to protect MOS
- Difficult to match C_{oss} of GaN and MOS
- Still has Q_{rr}

	GaNPower GaN HEMT	Super Junction MOS	SiC	Cascode GaN
Part ID	GPI65015TO	xxxxxxxxx	xxxxxxxxx	xxxxxxxxx
Rated Voltage	650V	700V	650V	600V
R_{on}	92mΩ	125mΩ	100mΩ	150mΩ
Q_g	3.3nC	35nC	51nC	6nC
$R_{on}*Q_g$	304	4375	5100	900

Cascode GaN HEMT

- Cascode can make package more complicated with 3 components and ceramic substrate
- Can be more expensive than pure E-mode
- Also, cascode is not feasible for low voltage (<200V) GaN, due to the R_{dson} portion from MOS is too high:
  - for 600V device, Rdson from MOS contribute less than 5%;
  - for 100V device, MOS can contribute more than 30% of the R_{dson}, which is impractical



1. System Plus Consulating: https://www.systemplus.fr
2. Alex Lidow Johan Strydom Michael de Rooij David Reusch, GaN TRANSISTORS FOR EFFICIENT POWER CONVERSION, Wiley

Commercial E-Mode GaN HEMT with "p-GaN"

Infineon Panasonic

GIT: Gate with Ohmic Contact and Current Control →

Conventional Gate Injection Transistor (GIT)

Source Gate P-GaN Drain
AlGaN
GaN
Buffer layer
Si - substrate

New hybrid-drain-embedded GIT (HD-GIT)

Source Gate P-GaN Drain
AlGaN
GaN
Buffer layer
Si - substrate

VisIC Technologies
GaN Systems
EPC EFFICIENT POWER CONVERSION
Navitas
GANPOWER INTERNATIONAL

Gate with Schottky Contact and Current Control →

Gate
p-GaN
Passivation
S
D
AlGaN Barrier
2DEG
GaN Buffer
Substrate

10^{0}, 10^{-2}, 10^{-4}, 10^{-6}, 10^{-8}, 10^{-10}, 10^{-12}
I_G (A)
GIT p-GaN
p-GaN
-15 -12 -9 -6 -3 0 3 6
V_{GS} (V)

1 , Kevin J. Chen, Understanding the Dynamic Behavior in GaN-on-Si Power Devices and IC's, Integrated Power Conversion and Power Management, 2018
2 , Greco, G., Iucolano, F., & Roccaforte, F. Review of technology for normally-off HEMTs with p-GaN gate. Materials Science in Semiconductor Processing

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Why no Avalanche Breakdown in GaN?

- GaN has a very high critical electric field (10 times that of Si, on par with SiO_2 or SiN already)
- Lateral device structure causes electric field crowding, particularly in overlying insulators
- GaN HEMT is more like a ceramic capacitor breakdown in the overlying insulators, where peak electric field took place
- If breakdown ever occurs, the device suffers permanent damage
- Design margin (>30%) for GaN is usually much higher than that of Si (which only has 10%)

1D Cut

E-Field

Elec Field Mag. (V/cm)

Potential

Differential Potential

SiN

AlGaN

GaN

Elec Field Mag. (V/cm)

Distance(um)

Elec Field Mag. (V/cm)

SiN

AlGaN

GaN

y(micron)

x(micron)

Michael A Briere, "Understanding The Breakdown Characteristics Of Lateral GaN-Based HEMTs"

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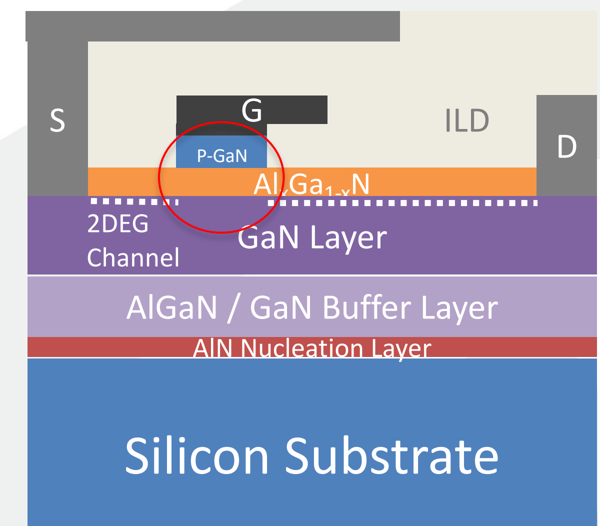
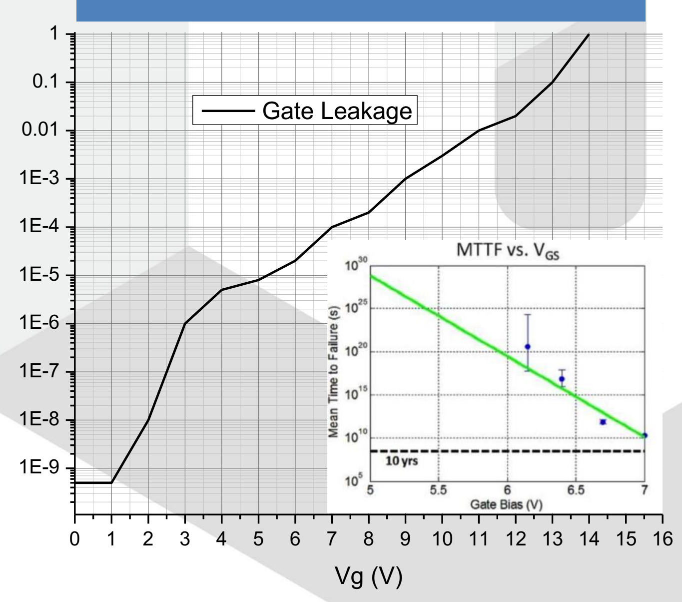
Why no P-type GaN HEMT Like PMOS?

- Si has both NMOS and PMOS, for NMOS, current is carried by electrons while in PMOS, current is carried by the holes
- However, for GaN HEMT, there is no P-type GaN HEMT yet
- First, ion implantation and subsequent annealing of magnesium in GaN is very difficult to achieve
- Second, hole mobility in GaN is very low (30 cm^2/Vs for holes vs. 2000 cm^2/Vs for electrons)
- GaN monolithic ICs are realized either by using complementary E-mode and D-mode GaN, or using E-mode GaN only

Why E-mode GaN $V_{g\text{-}max}$ is Limited to 7V

- Unlike a silicon MOS, the P-GaN / AlGaN / GaN can be viewed as a PIN diode structure with a depletion region
- With in-situ doped p-type dopant (Magnesium) for p-GaN layer, the depletion region extends over the thickness of the GaN 2DEG channel for V_g=0V, thus interrupts the channel below the gate region
- When a positive gate bias is applied, the 2DEG channel is re-established, yielding to on-state conditions
- Gate leakage current increases with increasing gate voltage. Voltage beyond 7V will results higher gate leakage current
- For the P-GaN / AlGaN / GaN gate stack, a TDDB (Time Dependent Dielectric Breakdown) needs to be analyzed for proper max gate voltage with long term reliability concerns
- It has been determined that maximum rating of 6~7V for p-GaN HEMT is most appropriate





Current Collapse Phenomenon

Filled
Empty
Polarization Charge
e-
G
SiN
S
D
Depletion region
$Al_{0.3}Ga_{0.7}N$
2DEG
GaN Buffer Layer
AlN Nucleation Layer
Silicon Substrate

I_d
Before Drain Voltage Stress
After Stress
V_d

At large negative gate bias, electrons from the gate or substrate may leak to the trap states close to the 2DEG channel, creating a "virtual gate" and modulate the depletion region

Current Collapse: TCAD Transient Simulation

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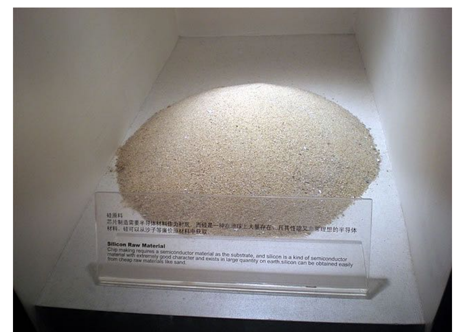
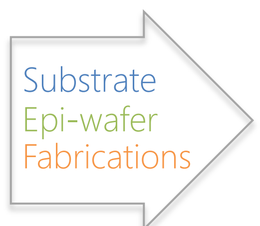
GaN Power Device Supply Chain



Basic Semiconductor Materials



GaNPower 6 inch GaN Wafer (real photo)

Packaging
Testing

Packaged GaN Devices

Final Power Supply Products

How GaN Power Devices Are Fabricated?

1 Epitaxial Wafer

1 Device Design and Layout

2 Device Fabrication

3 Circuit Probing (Wafer level testing)

4 New Lead frame Design

4 Packaging (Wire-bond)

4 Packaging (Bumping)

5 Final Testing (Packaging Level)

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GaN Design Stage (TCAD Simulation)

1 Device Design and Layout

S G D FEM_Structure

P-GaN HEMT Device Structure

FEM_Structure: Contact 3, Contact 2, Contact 1, GaN, SiN, AlGaN(x=0.26), AlGaN(x=0), AlGaN(x=0.05), AlGaN(x=graded) (2), AlGaN(x=graded) (1), Si

P-GaN, AlGaN, GaN, G, 2DEG, 1, 2

Device Structure Zoom-in

Simulated I_d-V_g Curve
V_{th} about 1.5V

Band diagram 1: V_{gs}@0V — P-GaN, AlGaN, GaN, Conduction Band, Fermi Level, Valence Band; Energy(ev); Distance(um)

Band diagram 2: V_{gs}@0V — 2DEG, Conduction Band, Fermi Level, AlGaN, GaN, Valence Band; Energy(ev); Distance(um)

Band diagram 1: V_{gs}@6V — 2DEG, P-GaN, Conduction Band, AlGaN, GaN, Quasi-Fermi Level, Valence Band; Energy(ev); Distance(um)

(*Simulated using Ohmic Gate Contact)

Simulated Using Crosslight NovaTCAD

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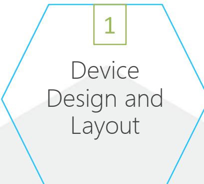
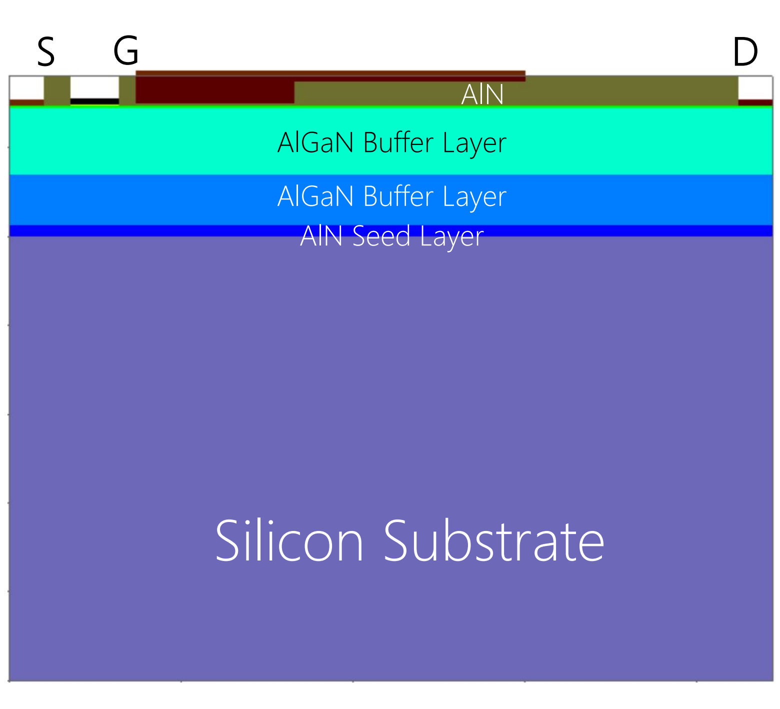
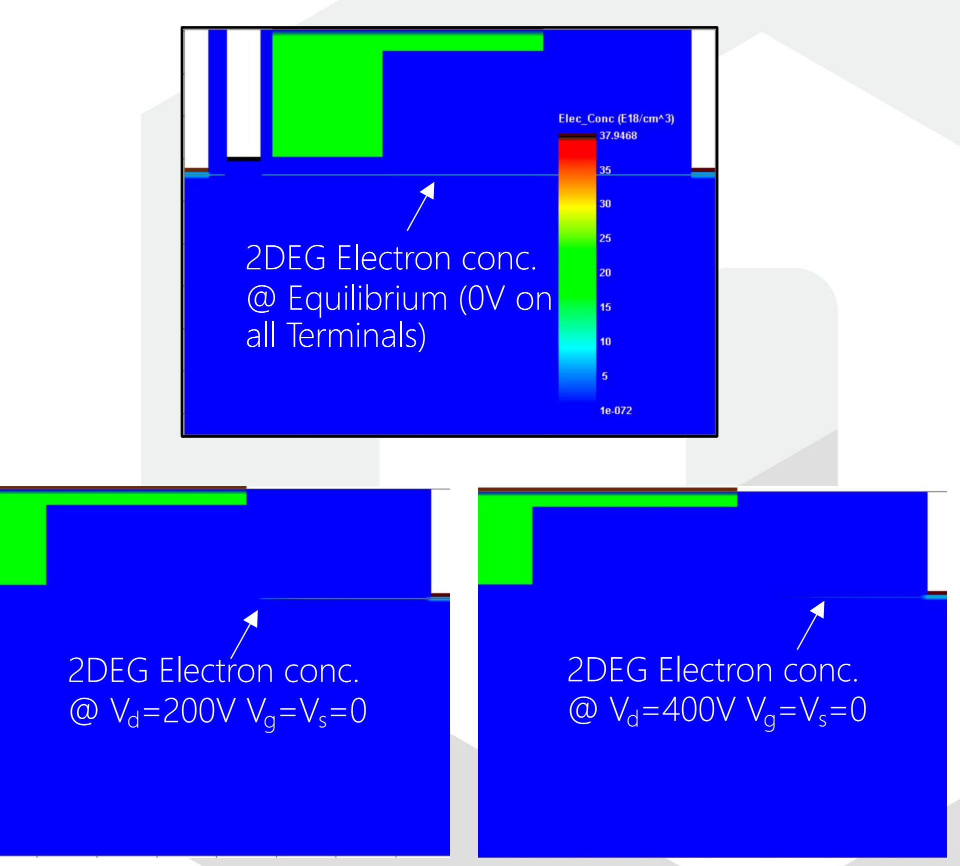
GaN Design Stage (TCAD Simulation)







Depletion Region Propagates

Simulated Using Crosslight NovaTCAD

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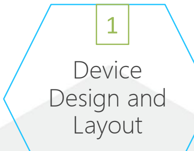
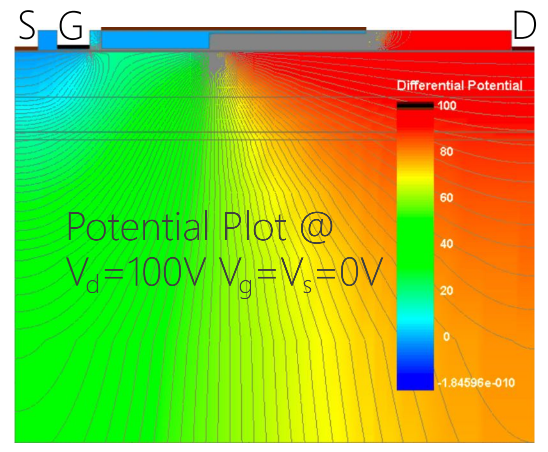
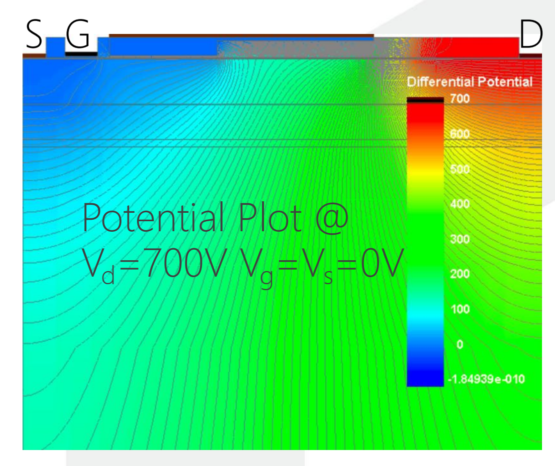
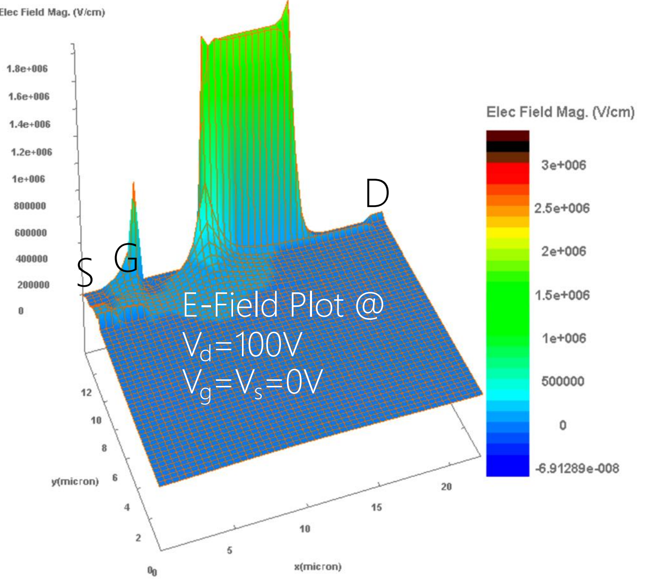
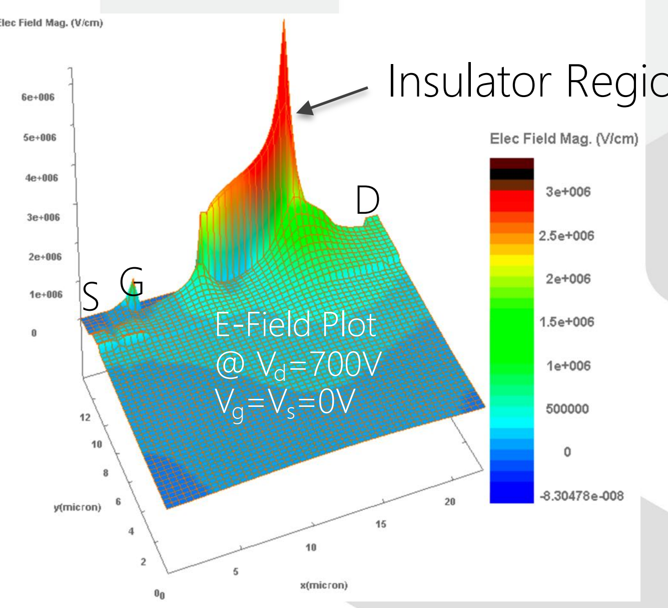


GaN Design Stage (TCAD Simulation)









Simulated Using Crosslight NovaTCAD

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Device Design and Layout

GaN Design Stage (TCAD Simulation)

SiN Layer

S_{xx} Compressive Stress

Stress_xx (GPa)

Drain Current (A/m)

Gate Voltage (V)

Without intrinsic stress

With SiN intrinsic stress (compressive)

- In addition to stress caused by material lattice mismatch, the intrinsic stress from SiN layer can be defined in the process simulation. The stress profile can be used by the device simulator to calculate the piezoelectric polarization.

- Stress engineering may help to achieve enhancement mode?

Simulated Using Crosslight NovaTCAD

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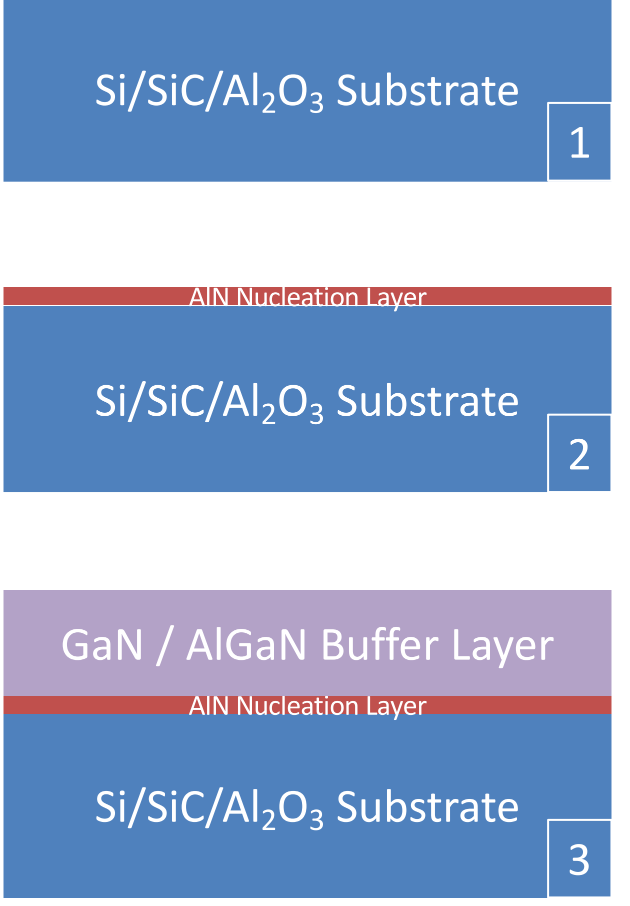
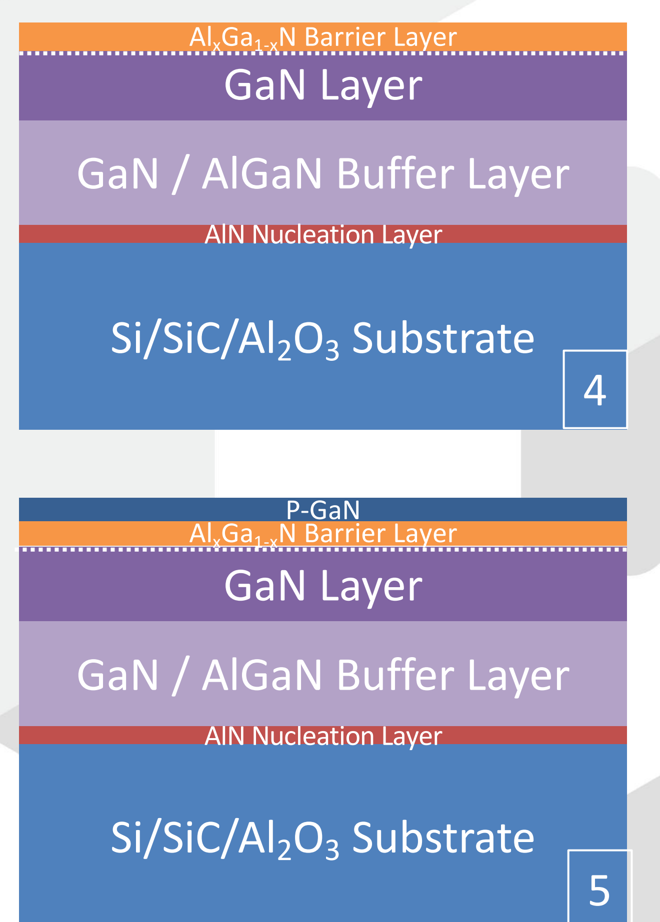
Fabrication Process Flow for GaN Epi-layer

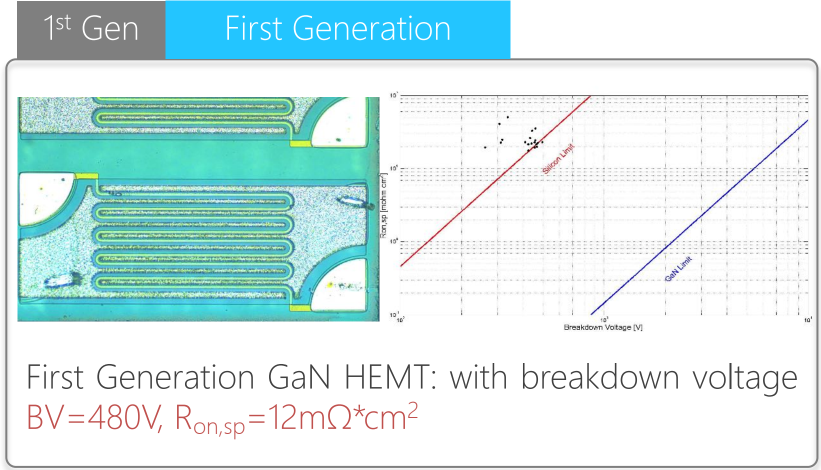
The GaN Epi wafer is fabricated from either Si, SiC or Sapphire substrate. Each layer is deposited using MOCVD (Metal Organic Chemical Vapor Deposition) for low cost and high throughput





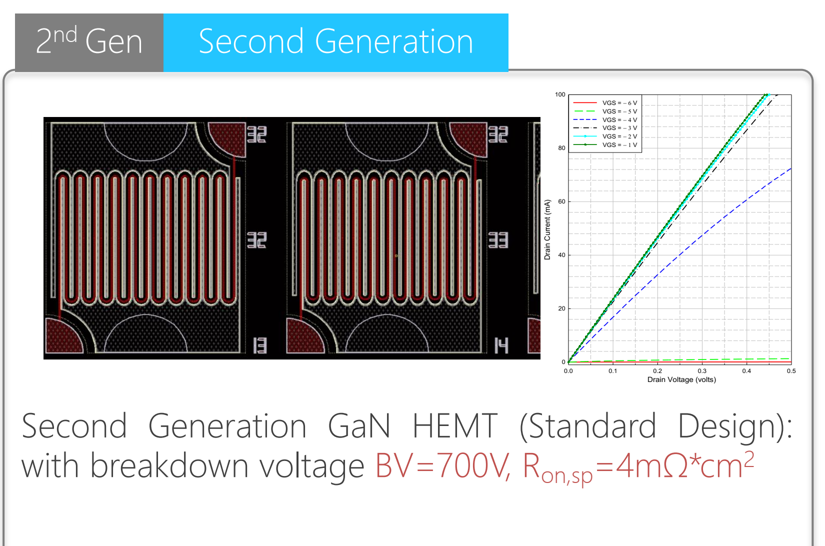
A GaN-on-Sapphire HEMT Fabrication Example

1st Gen First Generation



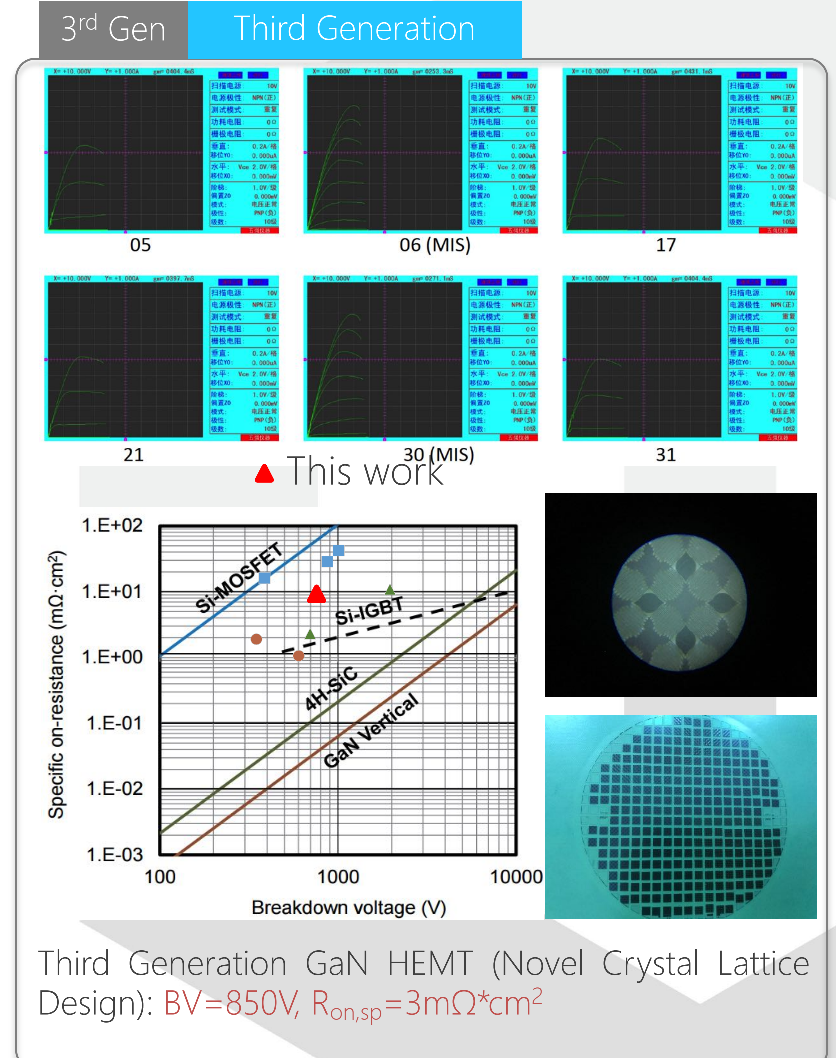
First Generation GaN HEMT: with breakdown voltage BV=480V, $R_{on,sp}$=12mΩ*cm²

2nd Gen Second Generation

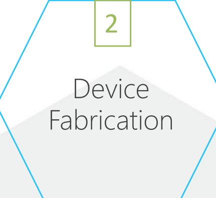


Second Generation GaN HEMT (Standard Design): with breakdown voltage BV=700V, $R_{on,sp}$=4mΩ*cm²

3rd Gen Third Generation



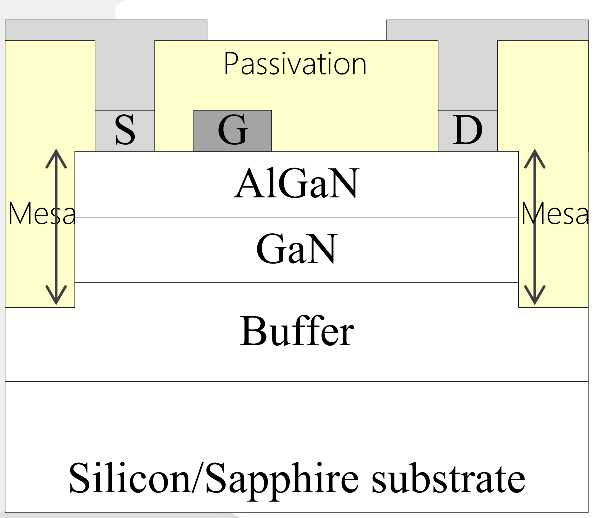
Third Generation GaN HEMT (Novel Crystal Lattice Design): BV=850V, $R_{on,sp}$=3mΩ*cm²



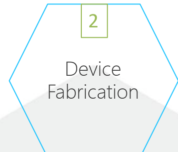
Fabrication Steps (D-mode HEMT)

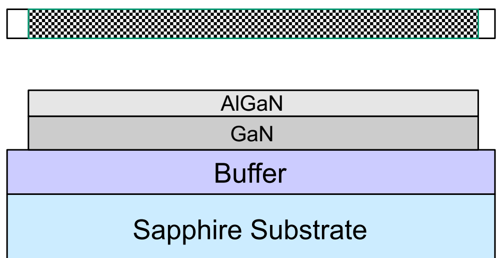
Simplified GaN-on-Sapphire HEMT Process Flow (GaN-on-silicon is similar):

1	Wafer Cleaning
2	Mask #1: Mesa Etching
3	RIE Mesa Etching
4	Mask #2: S/D Contacts
5	Ohmic Contact Deposition
6	Mask #3: Gate Lithography
7	Schottky Gate Deposition
8	Growth of Passivation Layer
9	Mask #4: Contact Hole Opening
10	Mask #5: Field plate and metallization



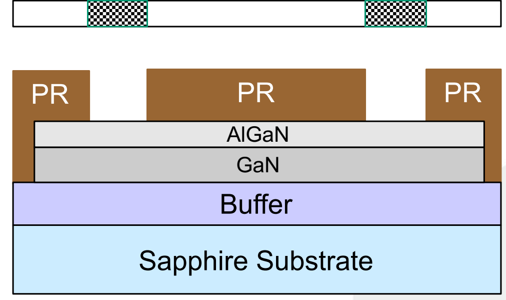
A GaN-on-Sapphire HEMT Process Flow Example





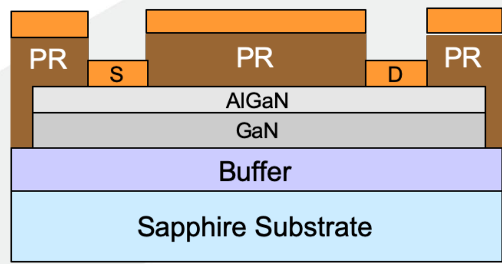
① Mask 01 – Mesa etch

- Define a device area
- Create isolation between devices



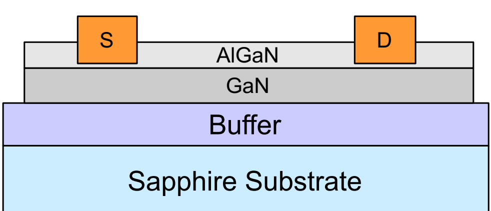
② Mask 02 – S/D

- Source and drain contact to AlGaN
- The metal must be deposited after a completely clean process to eliminate layers between AlGaN and Metal



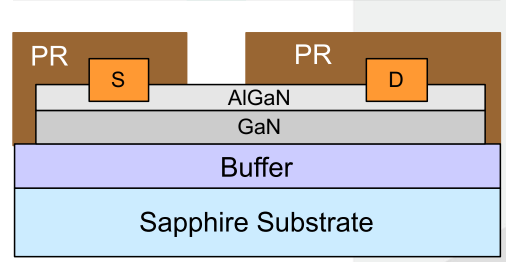
③ Deposit S/D metal

- Deposit ohmic contacts on top of AlGaN as source and drain



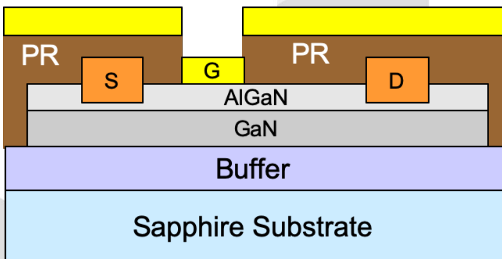
④ Lift-off and Anneal

- To improve contact quality
- Bad annealing may dramatically degrade the device performance



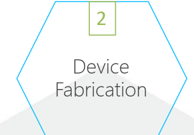
⑤ Mask 03 – Gate

- Define gate region
- The alignment in this step is the most critical as it affects many parameters (L_{gd}, Gate on Mesa, design of field plate)

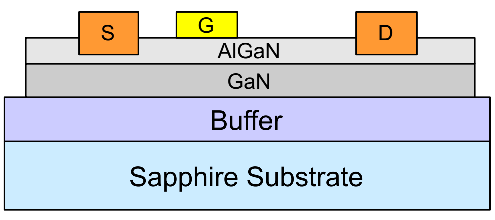


⑥ Gate Metal Deposition

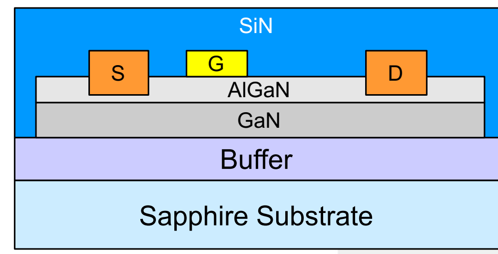
- Pre-clean is important for the Schottky barrier



A GaN-on-Sapphire HEMT Process Flow Example

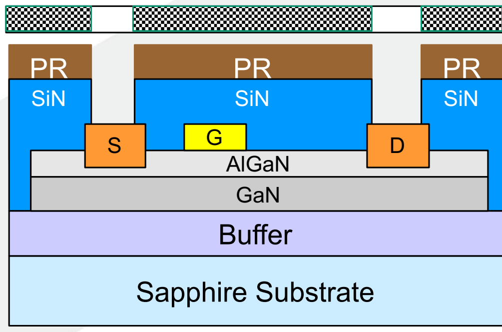


⑦ Gate metal Lift-off



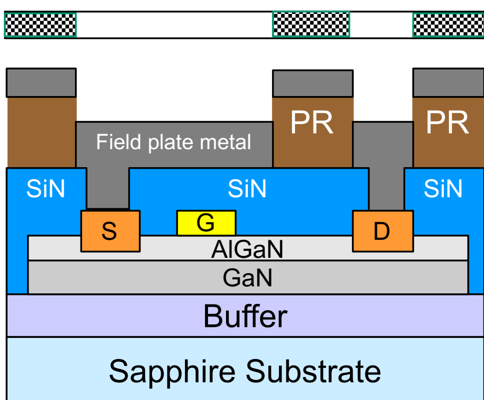
⑧ SiN deposition (passivation)

- The first layer of SiN layer is for passivation
- It is important for decreasing the traps at the AlGaN surface
- Many device performances, including leakage current, threshold voltage, breakdown voltage, are related to the quality of this passivation
- This layer is also used for the field plates

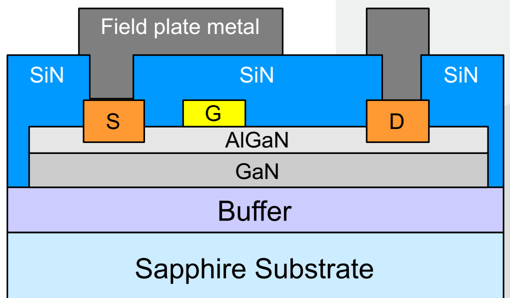


⑨ Mask 04: S/D contact

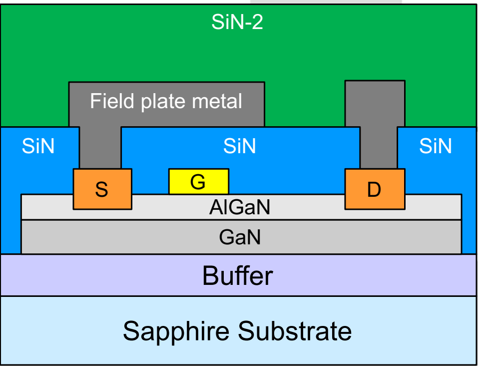
- The source fingers are opened for field plates
- The S/D/G pads are opened
- All other area should be covered by SiN



⑩ Mask 05 – Field Plate



⑪ Field Plate Lift-off

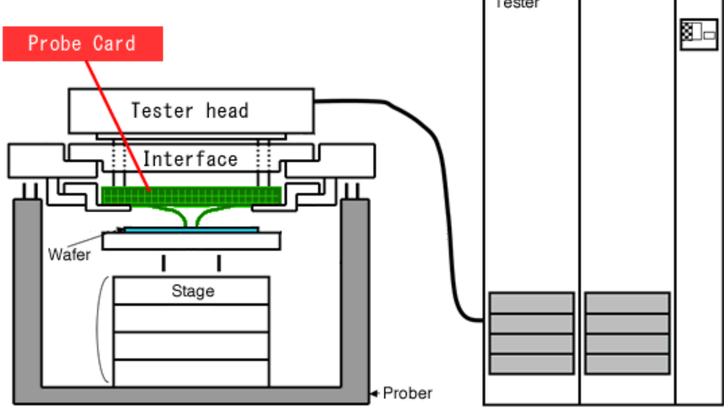


⑫ Second SiN deposition

- covers the whole area

Circuit Probing (Wafer level testing)

Circuit Probing (CP)



Probe Card

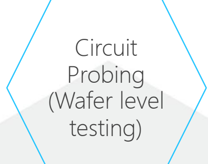
https://www.mjc.co.jp/en/technology/
http://www.jemam.com/probecard.htm
https://www.formfactor.com/
http://www.jem-net.co.jp/en/products/pro_hando_top.html

Circuit Probing can sort out bad dies from good dies by combining multiple test items, both room temperature and high temperature tests can be applied

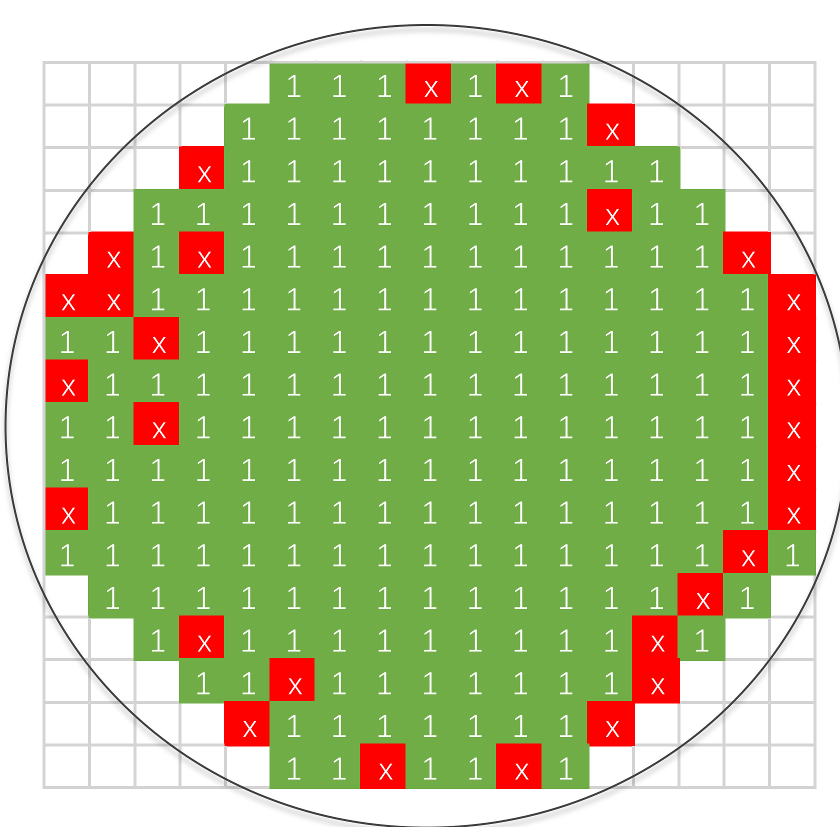
Test items example:

- ✓ I_{dss}: Drain leakage current
- ✓ I_{gss}: Gate leakage current
- ✓ V_{th}: Threshold voltage
- ✓ R_{dson}: On-state resistance
- ✓ g_m: Transconductance

Pass / Fail depends on specified range, bad dies are inked to avoid being picked up for further packaging



Circuit Probing (CP)



Failed sites are marked with ink and will not be picked for packaging afterwards

In this example, we have:

- ✓ Total dies: 229
- ✓ Bad dies: 32
- ✓ Yield: 86%

Sometimes the CP specs are too tight, resulting lower yield. But a too loose spec can lead to increased device early failures

Simplified Packaging Steps

Probe Card
Tester head
Interface
Wafer
Stage
Prober
Tester
Circuit Probe

Wafer IQC

Taping

Turn over the surface of wafer

Wafer BG

De-Taping

BSM Evaporation (option)

BSC Laminating (option)

Laser Marking

Mounting

Low-k Grooving (option)

Dicing

AOI

Silicon Die
Wedge Bond
Aluminium Wire
Source Connection
Gate Connection
Copper Tab (Drain Connection)
Wire Bond

Tape & Reel

Tape Running Direction
Automatic microscope
IC
Visual Inspection

Label
Shielding
Reel
Package

Final Test (FT)

Power device FT tester

Final test can identify problems with assembled devices, and it is the last test before shipment

Test items example:

- ✓ I_{dss}: Drain leakage current
- ✓ V_{th}: Threshold voltage
- ✓ R_{dson}: on-state resistance
- ✓ BV: Breakdown voltage

Pass / Fail depends on specified range

http://www.accotest.com/index.asp

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GaN Packaging Types

DFN 8x8

DFN 6x8

LGA

TO 252

TO 220

Infineon

CoolGaN™

600 V e-Mode

GaN

GS61004B

(e4)

GaN Device Parameter Testing

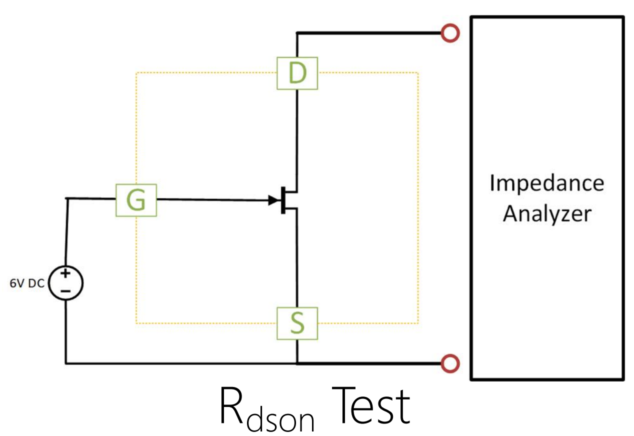
- ✓ Static (DC) parameters testing
  - ➢ R_{dson}, V_{th}, BV, I_{dss}, I_{gss}, V_{sd}, R_g, etc…
- ✓ Dynamic parameters testing
  - ➢ C_{iss}, C_{rss}, C_{oss}, Q_g, Q_{gs}, Q_{gd}, Q_{rr}, etc…
- ✓ Double pulse testing (for dynamic parameters)
  - ➢ T_r, T_f, T_d, dv/dt, etc…
- ✓ Thermal testing
  - ➢ R_{thjc}, R_{thja}, etc…
- ✓ SOA testing

Parameter Testing: DC Parameters

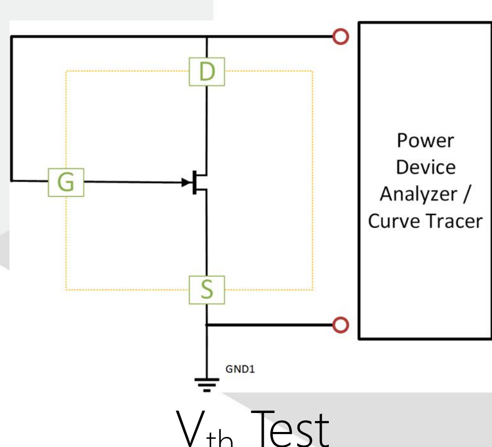
✓ Static (DC) parameters testing for GaN HEMTs

- R_{dson} is tested by applying a 6V gate bias, Kelvin connection should be applied if an impedance analyzer or a power device analyzer/curve tracer such as Keysight 1505A is used. Both room and high temperature R_{dson} can be recorded at certain drain current level (e.g. I_d=5A for 100 mΩ device)

- V_{th} is tested by shorting drain and gate terminals and apply a voltage to the drain with respect to the source. The voltage is recorded at certain drain current level (e.g. 3.5 mA for 100 mΩ)



R_{dson} Test



V_{th} Test

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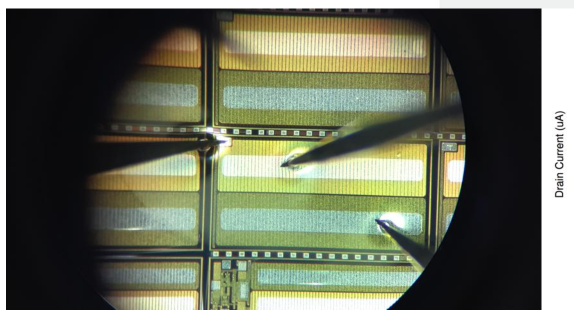
Parameter Testing: DC Parameters

✓ Static (DC) parameters testing for GaN HEMTs

- BV (breakdown voltage test) for GaN HEMT is very different from MOSFET. For I_d-V_d breakdown curves are rarely seen in the datasheet. Unlike silicon MOSFET, GaN doesn't have avalanche breakdown. Once GaN device breakdown, the device is destroyed, and the equipment is likely not fast enough to catch the complete curves

- GaNPower's 650V E-mode devices real breakdown voltage is above 900V for a safety margin

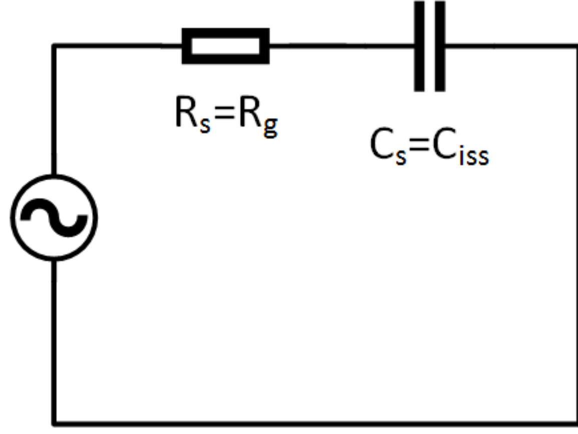
- GaNPower is also the world's first and only provider of 1200V single chip E-mode GaN HEMT, with real breakdown voltage exceeding 1500V



E–mode GaN HEMT 1200V/15A, IdVd at Vg=0
Device 1
Device 2
Device 3
Drain Current (uA)
Drain Voltage (V)

Parameter Testing: R_g

Gate internal resistance is measured with drain open and high frequency, such as f=25MHz

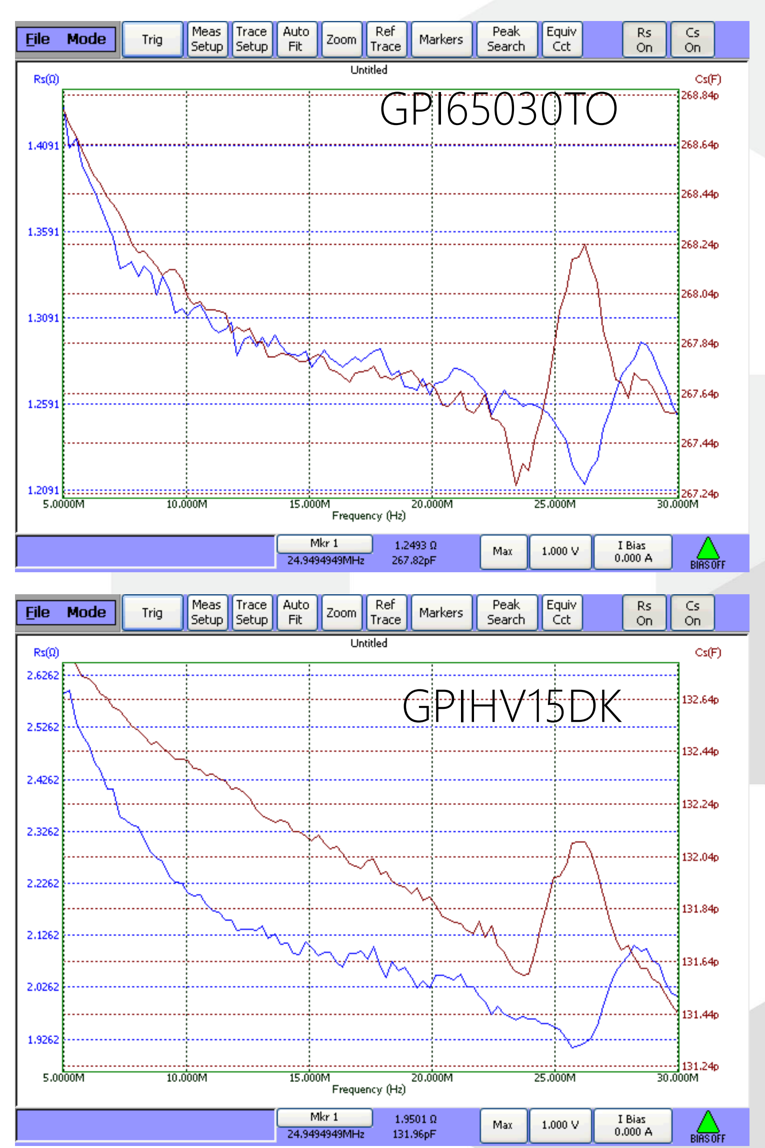


$$V(t) = V_{bias} + V_o \sin \omega t$$

$$I(t) = I_o \sin(\omega t + \theta)$$

$$I_o = \frac{V_o}{\sqrt{R^2 + (\frac{1}{\omega C})^2}}$$

$$\theta = \tan^{-1} \frac{1}{R\omega C}$$



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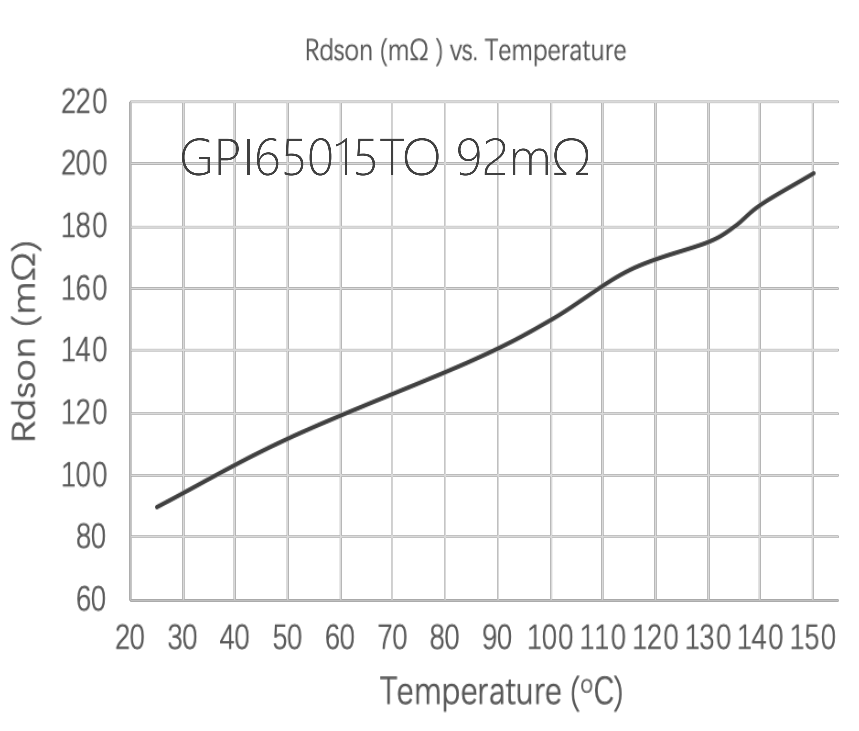
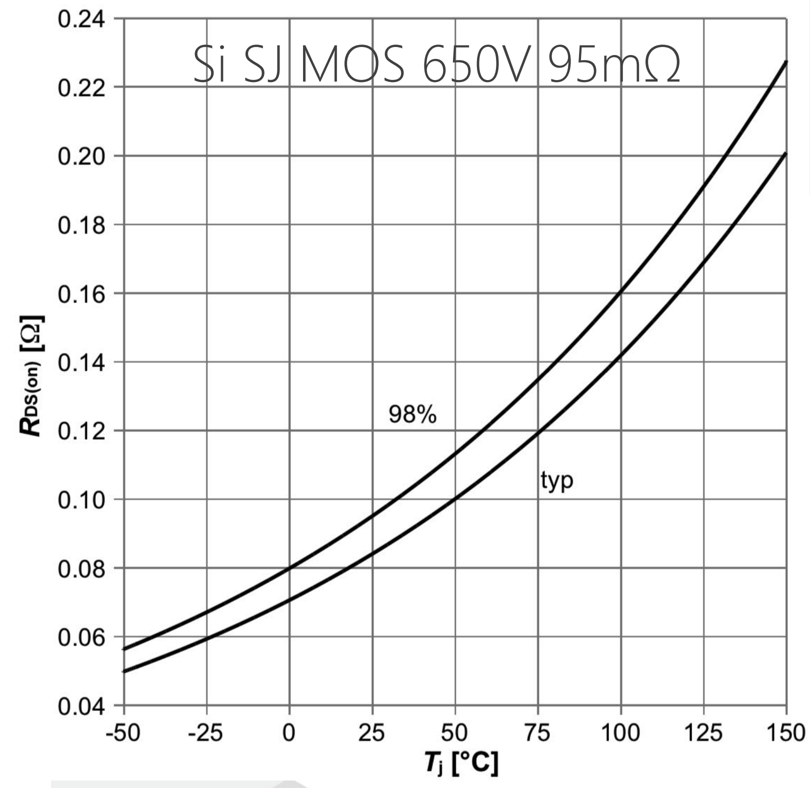
Parameter Testing: R_{dson} vs. Temp





For GaN HEMT: R_{dson} temp ratio: $R_{dson(T=25C)}$/ $R_{dson(T=150C)}$ =195mΩ/92mΩ=2.12

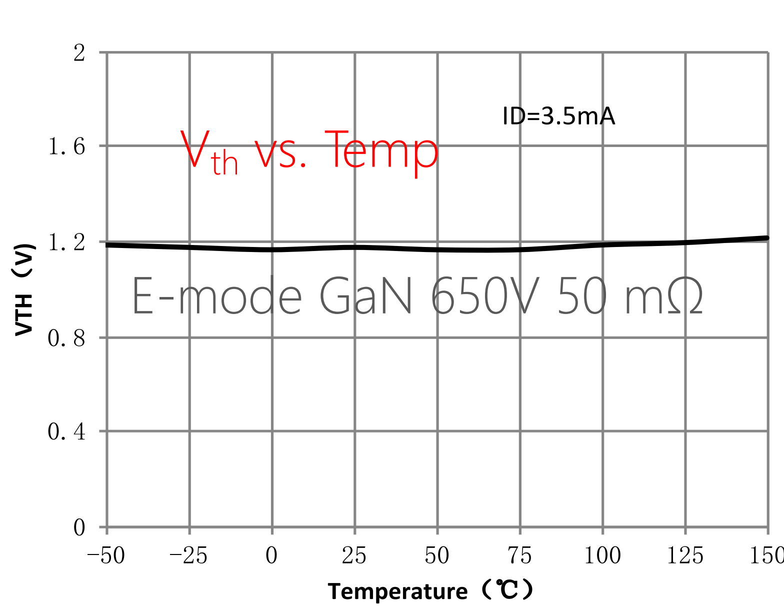
For SJ MOS: R_{dson} temp ratio: $R_{dson(T=25C)}$/ $R_{dson(T=150C)}$ =200mΩ/90mΩ=2.17

R_{dson} temperature ratio of GaN HEMT and SJ MOS are on par

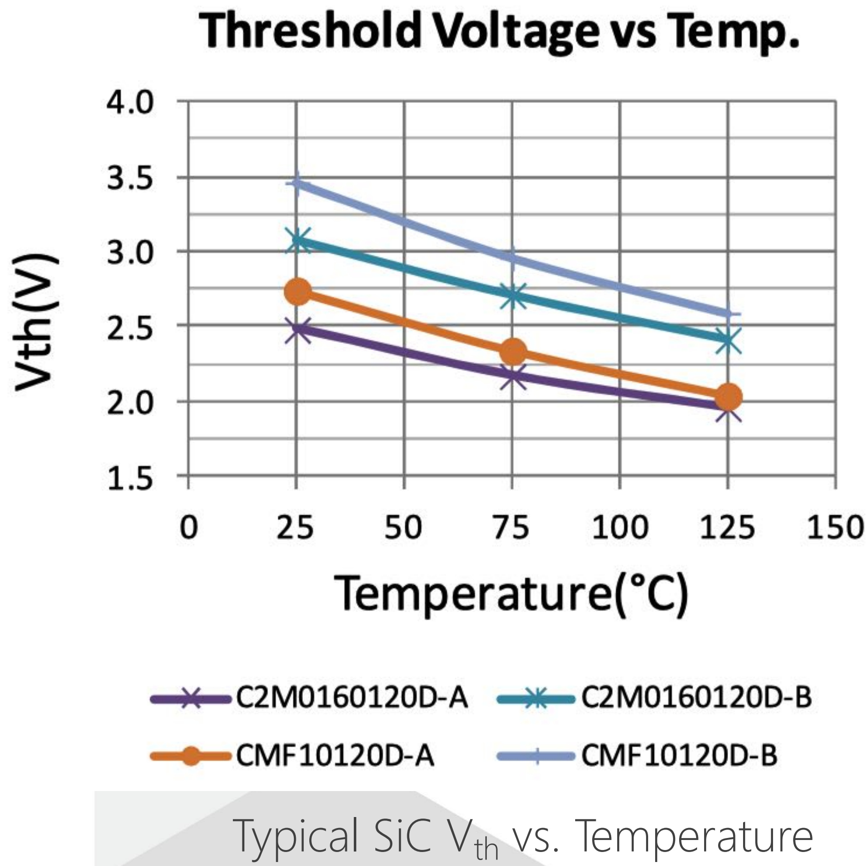
Parameter Testing: I_D vs. V_{GS}

For silicon SJ MOS, a Zero Temperature Coefficient (ZTC) point exists. Below this point, current increases with increasing temperature, causing hot spot and device failure. E-mode GaN has no such issue

Parameter Testing: V_{th} vs. Temp



Typical GaN V_{th} vs. Temperature



Typical SiC V_{th} vs. Temperature

Gangyao Wang, John Mookken, Julius Rice, Marcelo Schupbach: Dynamic and Static Behavior of Packaged Silicon Carbide MOSFETs in Paralleled Applications , IEEE https://www.richardsonrfpd.com/docs/rfpd/Dynamic_and_Static_Behavior_SiC_MOSFET.pdf

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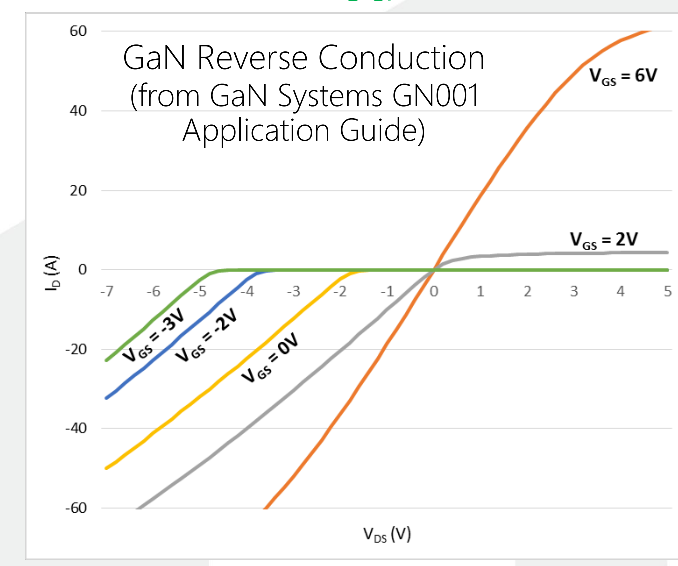
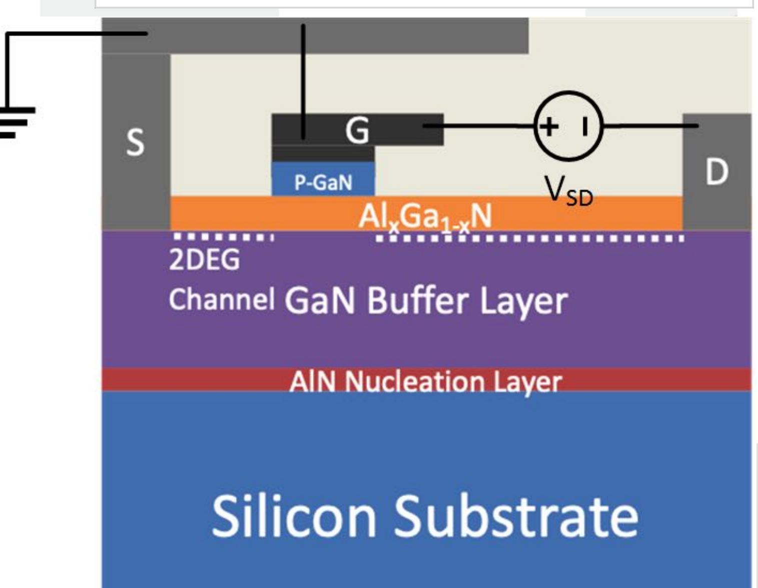
Parameter Testing: Reverse Cond. and V_{sd}

- There is no PN junction in the GaN device
- With S and G connected, applying a negative V_{DS} equals to applying a positive V_{GD}
- When V_{GD} exceeds the threshold voltage, the channel will conduct current, much like the body-diode of a MOSFET
- A negative bias on the Gate terminal requires an equal potential drop on the drain terminal so that V_{GD} can reach V_{th}
- In datasheet, V_{sd} is usually larger than V_{th} because the test criteria of I_d (for V_{th}) and I_s (for V_{sd}) is different. V_{sd} is usually defined at a much higher current value than V_{th}





Parameter Testing: Capacitance

C_{GS}

Field Plates

C_{DS}

S

G

P-GaN

D

C_{GD}

C_{GS}

AlN Nucleation Layer

Silicon Substrate

C_{DSub}

$C_{iss} = C_{GS} + C_{GD}$

$C_{oss} = C_{DS} + C_{GD}$

$C_{rss} = C_{GD}$

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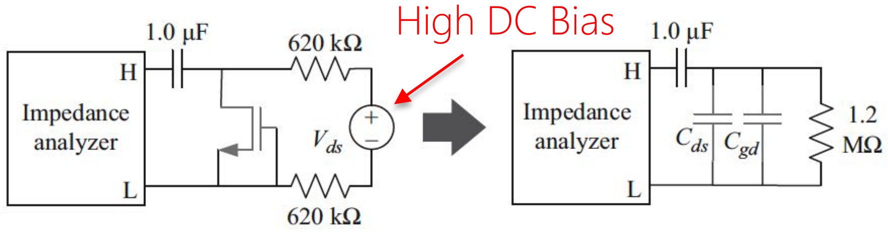
Parameter Testing: Capacitance

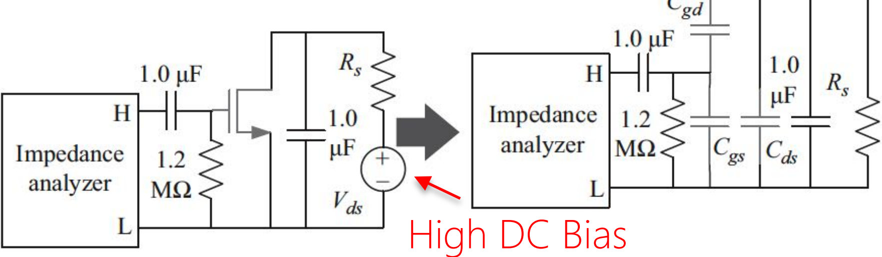


(a) Test setup for GaN HEMT C_{oss}

$$C_{oss} = \frac{C_{isolation}C_{measured}}{C_{isolation} - C_{measured}}$$

$$C_{measured} \ll C_{isolation} = 1uF;\ \ C_{measured} \sim pF\ range$$

$$C_{oss} \approx C_{measured}$$

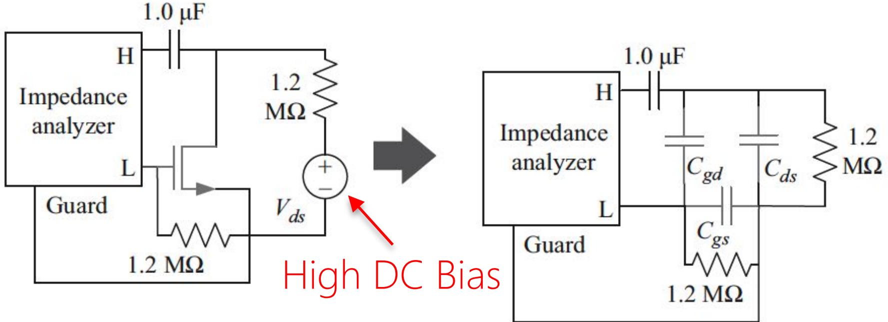


(b) Test setup for GaN HEMT C_{iss}

$$C_{iss} = \frac{C_{isolation}C_{measured}}{C_{isolation} - C_{measured}}$$

$$C_{measured} \ll C_{isolation} = 1uF;\ \ C_{measured} \sim pF\ range$$

$$C_{iss} \approx C_{measured}$$



(c) Test setup for GaN HEMT C_{rss}

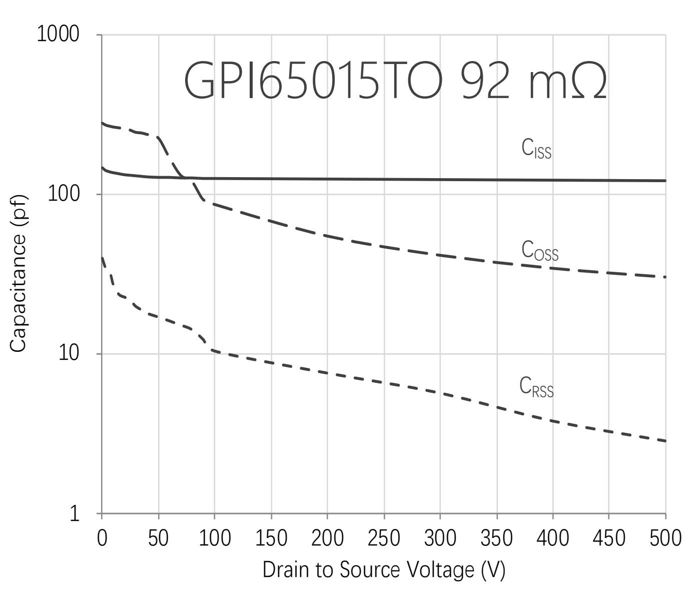
$$C_{rss} = \frac{C_{isolation}C_{measured}}{C_{isolation} - C_{measured}}$$

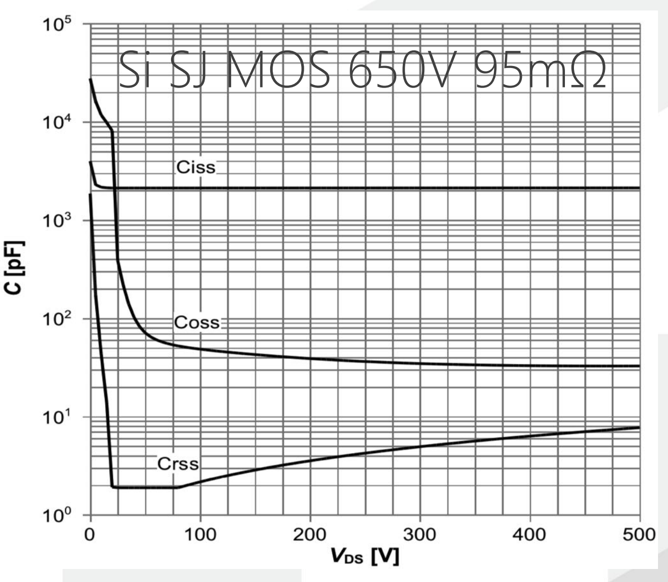
$$C_{measured} \ll C_{isolation} = 1uF;\ \ C_{measured} \sim pF\ range$$

$$C_{rss} \approx C_{measured}$$

Fei (Fred) Wang, Zheyu Zhang, and Edward A. Jones: Characterization of Wide Bandgap Power Semiconductor Devices, The Institution of Engineering and Technology 2018

Capacitance: Si SJ MOS vs. GaN





For GaN HEMT: C_{OSS} variation: $C_{oss(Vds=0.5V)}/C_{oss(Vds=500V)}$=521pF/30pF=17.4

For Si SJ MOS: C_{OSS} variation: $C_{oss(Vds=0.5V)}/C_{oss(Vds=500V)}$=2.8X$10^4$pF/32pF=875

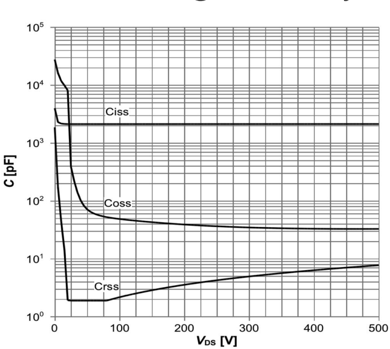
Silicon SJ MOSFET has a much wider C_{oss} variation, which causes significant non-linearity -> more severe EMI

Super Junction MOS C_{DS} Non-linearity

- C_{ds} can be calculated as:

$$C_{ds} \propto \frac{\varepsilon A}{d}$$

- A is the total area formed by the P/N junction depletion region, d is depletion width
- For small V_{ds}, A is large, and d is narrow, so C_{ds} is large
- With increasing V_{ds}, d increases while A keeps almost constant, C_{ds} decreases
- At certain V_{ds}, the lateral depletion regions merge, A suddenly drops, and d is wide, C_{ds} decreases significantly



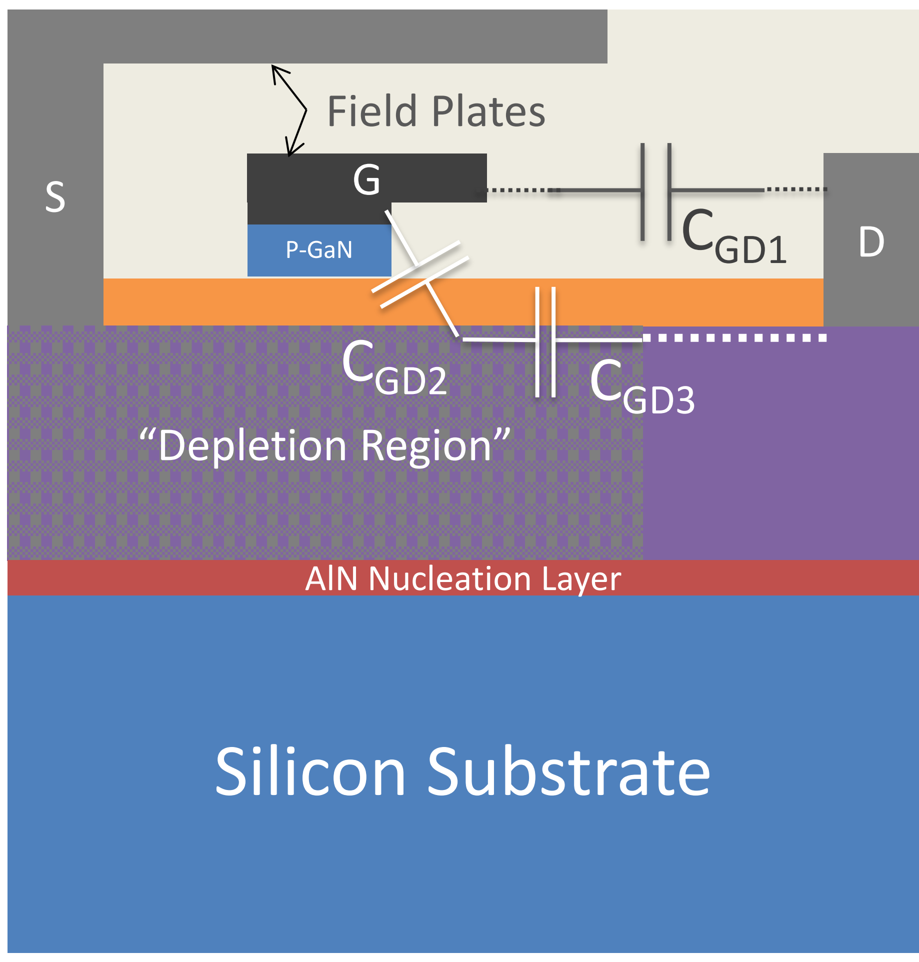
Source/Body Metal
N+ Gate N+
P+ P+
P-Body P-Body
P-Col C_{ds} N-Drift P-Col
N+ Substrate
Drain

Source/Body Metal
N+ Gate N+
P+ P+
P-Body P-Body
P-Col d Depletion region N-Drift (V_{ds}=0V) Depletion region P-Col
N+ Substrate
Drain

Source/Body Metal
N+ Gate N+
P+ P+
P-Body P-Body
P-Col d Depletion region N-Drift (V_{ds}=10V) Depletion region P-Col
N+ Substrate
Drain

Source/Body Metal
N+ Gate N+
P+ P+
P-Body P-Body
P-Col d Depletion Region (V_{ds}=400V) P-Col
N+ Substrate
Drain

GaN C_{GD} Non-linearity

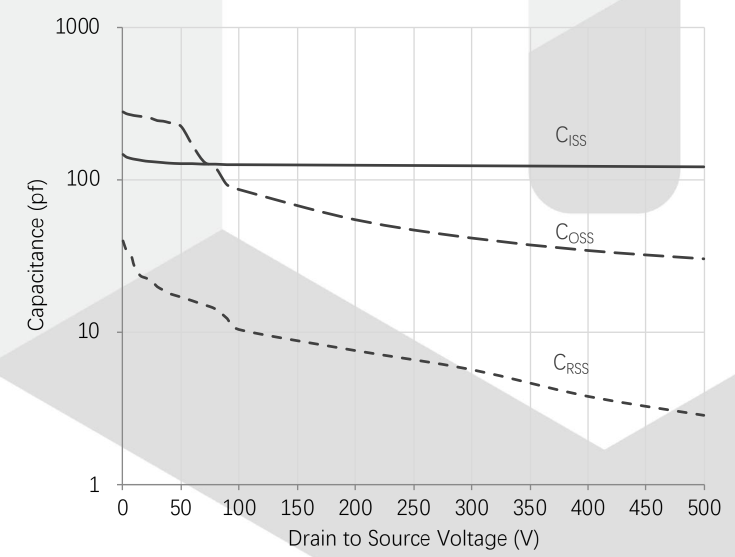


The nonlinearity of GaN is much smaller than SJ MOS in terms of C_{GD} and C_{DS}

- C_{GD} of GaN can be viewed as C_{GD2} and C_{GD3} in series and C_{GD1} in parallel:

$$C_{GD} = C_{GD1} + \frac{C_{GD2}C_{GD3}}{C_{GD2} + C_{GD3}}$$

- With a high V_{DS} applied, while C_{GD1} and C_{GD2} are not sensitive to V_{DS}, C_{GD3} decreases with the increasing depletion region, causing C_{GD} to decreases



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Capacitance: $C_{o(er)}$ and $C_{o(tr)}$

- C_{oss} is voltage dependent, no matter GaN or SJ MOS
- Single point C_{oss} value is not very useful, it can't represent the entirety of the capacitance curve
- By using the energy and time related effective output capacitance values, calculations will be more accurate, and they are more convenient to use
- These output capacitances ($C_{o(er)}$ and $C_{o(tr)}$) are usually evaluated at 80% of rated breakdown voltage (80% BVdss, or $BV_{80\%}$)
- The energy related effective output capacitance $C_{o(er)}$ and time related effective output capacitance $C_{o(tr)}$ can be calculated using the following equations:

$$C_{o(tr)} = \frac{Q_{oss-80\%}}{BV_{80\%}} = \frac{\int_0^{BV_{80\%}} C(V)dV}{BV_{80\%}}$$

$$C_{o(er)} = \frac{2}{BV_{80\%}^2} = \int_0^{BV_{80\%}} C(V)VdV$$

Alexander J. Young, ON Semiconductor, Characterizing the dynamic output capacitance of a MOSFET

Parameter Testing: Q_g

- Q_g can be tested with single pulse inductive load switching
- The value of R_G is intentionally chosen to be large (>300Ω) so that the switching transient can be slowed down for better calculation
- Q_g can then be extracted as (for Turn-off):

$$I_G(t) = \frac{V_G(t) - V_{G-applied}(t)}{R_G}$$

$$Q_G(V_G) = \int_0^t \frac{V_G(t) - V_{G-applied}(t)}{R_G} dt$$

$$Q_{GS} = Q_G\ (V_G = V_{Plateau})$$

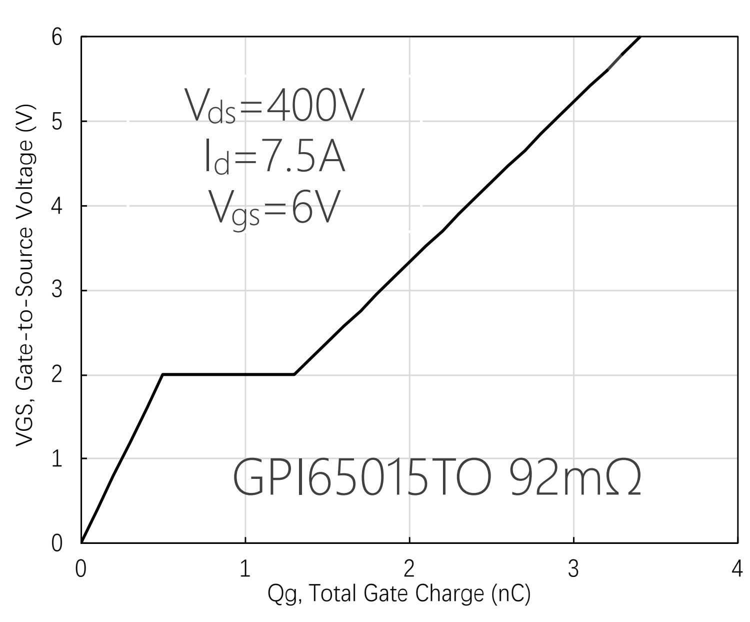
$$Q_{GD} = Q_{G(V_D=0)} - Q_{G(V_D=VDD)}$$

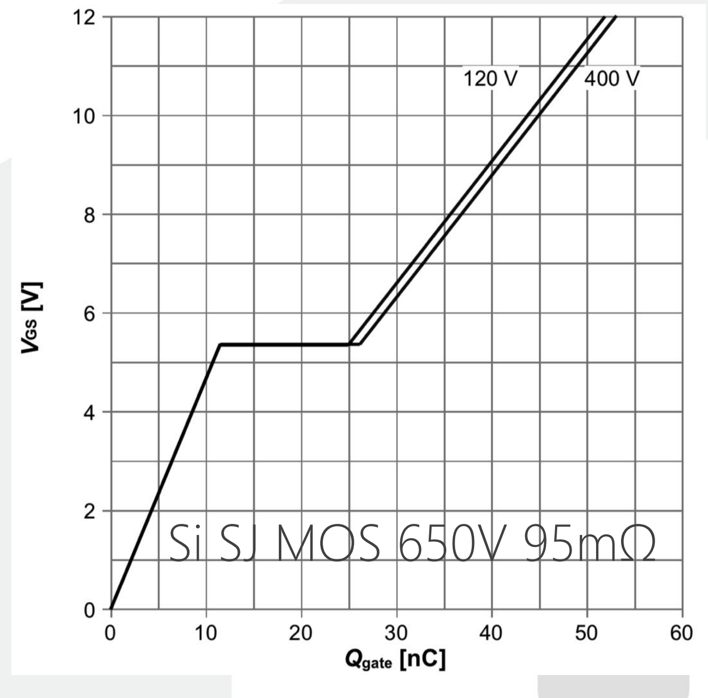
L
C_{IN}
V_{DD}
V_G
DUT
$V_{G\text{-applied}}$
R_G

V_{gs}
I_{ds}
V_{ds}

V_{gs}
Q_G
Q_{GS}
Q_{GD}
Q_{GS1} Q_{GS2}
Q_G
Q_{GD}
Q_{GS}
Q_{GS1} Q_{GS2}

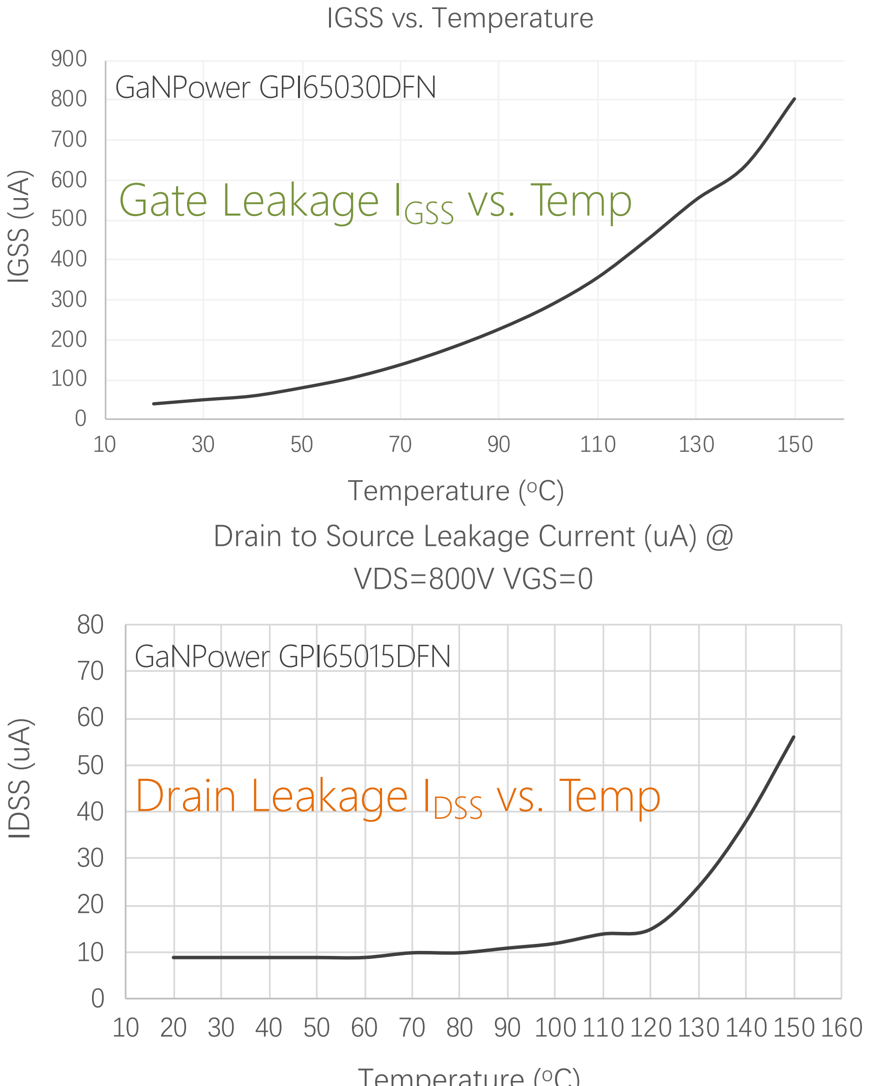
Parameter Testing: Q_g Curve

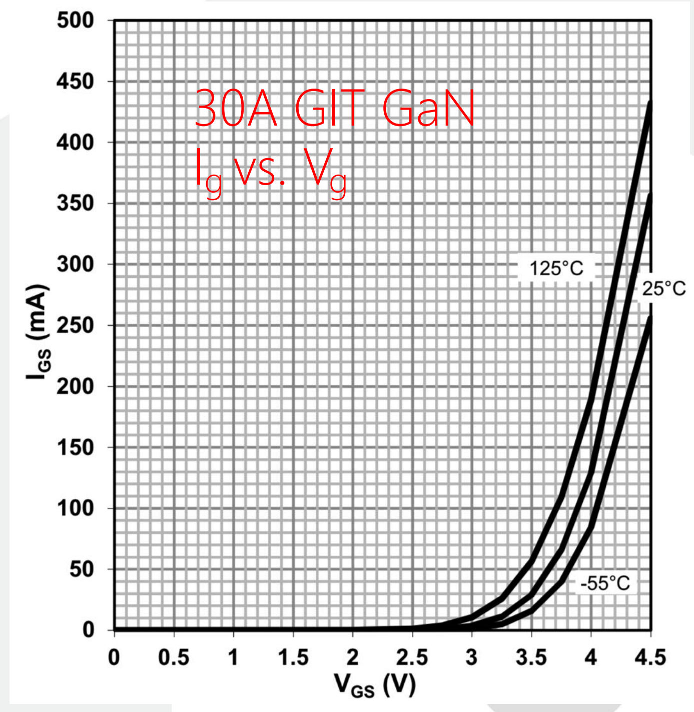




GaN Q_g is one order of magnitude smaller compared to silicon SJ MOS with similar R_{dson} and BV ratings

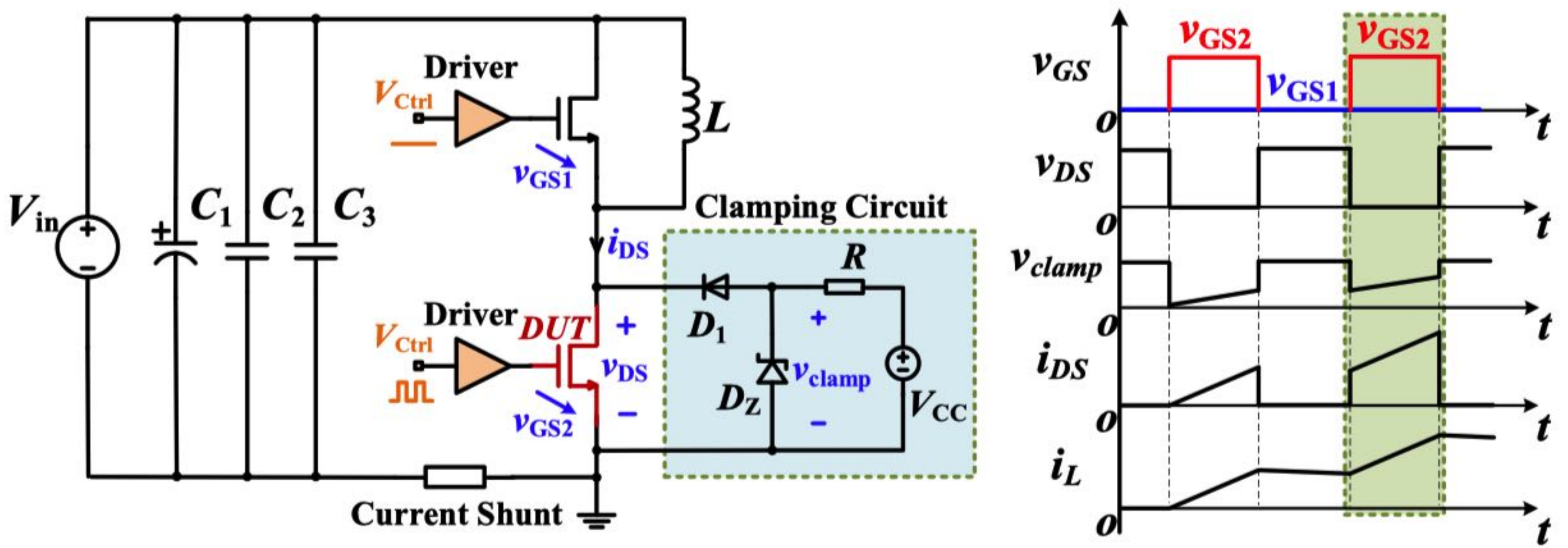
Parameter Testing: I_{dss} and I_{gss} vs. Temp.





- A GIT device, such as GaN offered by Panasonic and Infineon, exhibits a much higher gate current, since they are current driven, rather than voltage driven GaN devices, like BJTs

Current Collapse: Dynamic R_{dson}

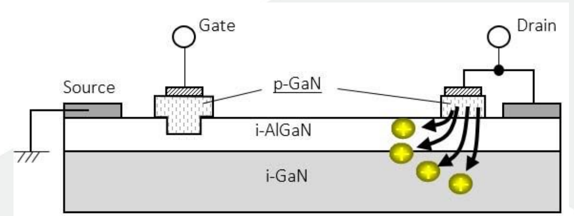


- There are various ways to measure dynamic R_{dson}, most of these methods involve a fast and accurate clamping circuit
- In this setup, the voltage drop V_{clamp} across the Zener diode D_Z is measured instead of V_{DS}, the diode forward voltage V_{D1} is calibrated so that low R_{dson} of GaN can be accurately measured
- R is chosen to limit the current of D_1 so that it won't heat-up

Source: Rui Li, Xinke Wu, Gang Xie, Kuang Sheng, Dynamic On-state Resistance Evaluation of GaN Devices under Hard and Soft Switching Conditions, APEC 2018

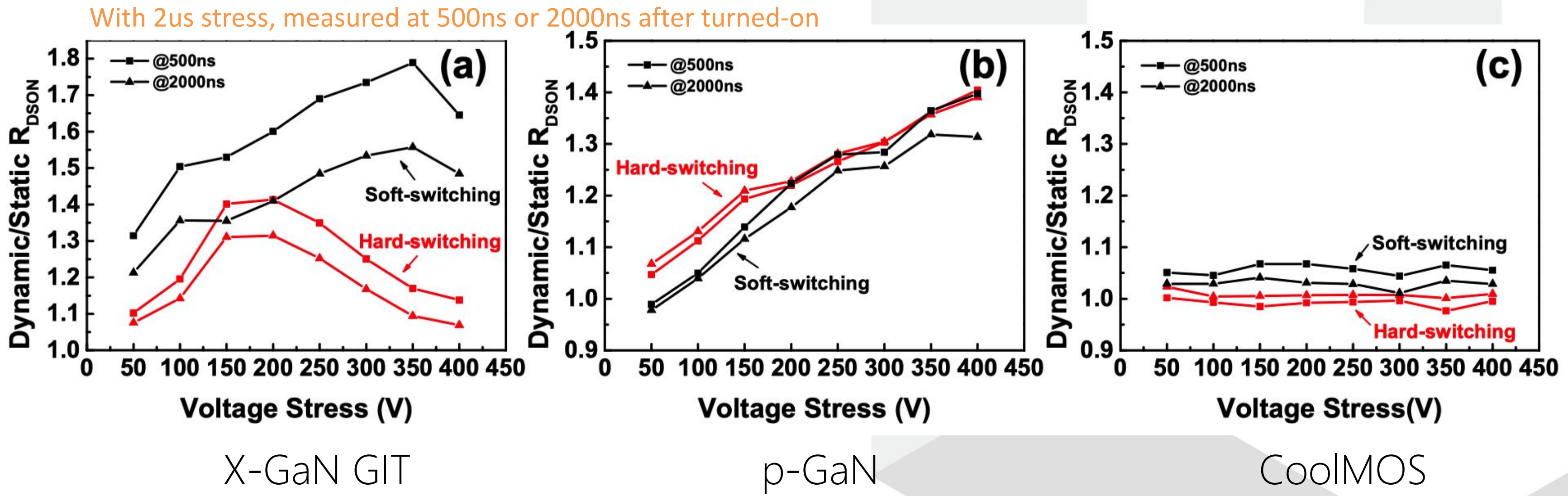
Current Collapse: Dynamic R_{dson}

Parameters	Device A	Device B	Device C
Voltage/Current Rating	600V/13A	650V/30A	600V/35A
Technology	E-mode (X-GaN GIT)	E-mode (p-gate)	CoolMOS™
Package	DFN 8×8	GaNPX™ 4	TO-220
R_{DSON}[a]	140mΩ	50mΩ	60mΩ



hybrid-drain- embedded-GIT. The hole injection from the additional drain-side p-GaN at the OFF state compensates the electron trapping in the epilayer. Successfully suppressed current collapse up to 850 V was obtained. (K.Chen IEEE TED 2017)

With 2us stress, measured at 500ns or 2000ns after turned-on



X-GaN GIT p-GaN CoolMOS

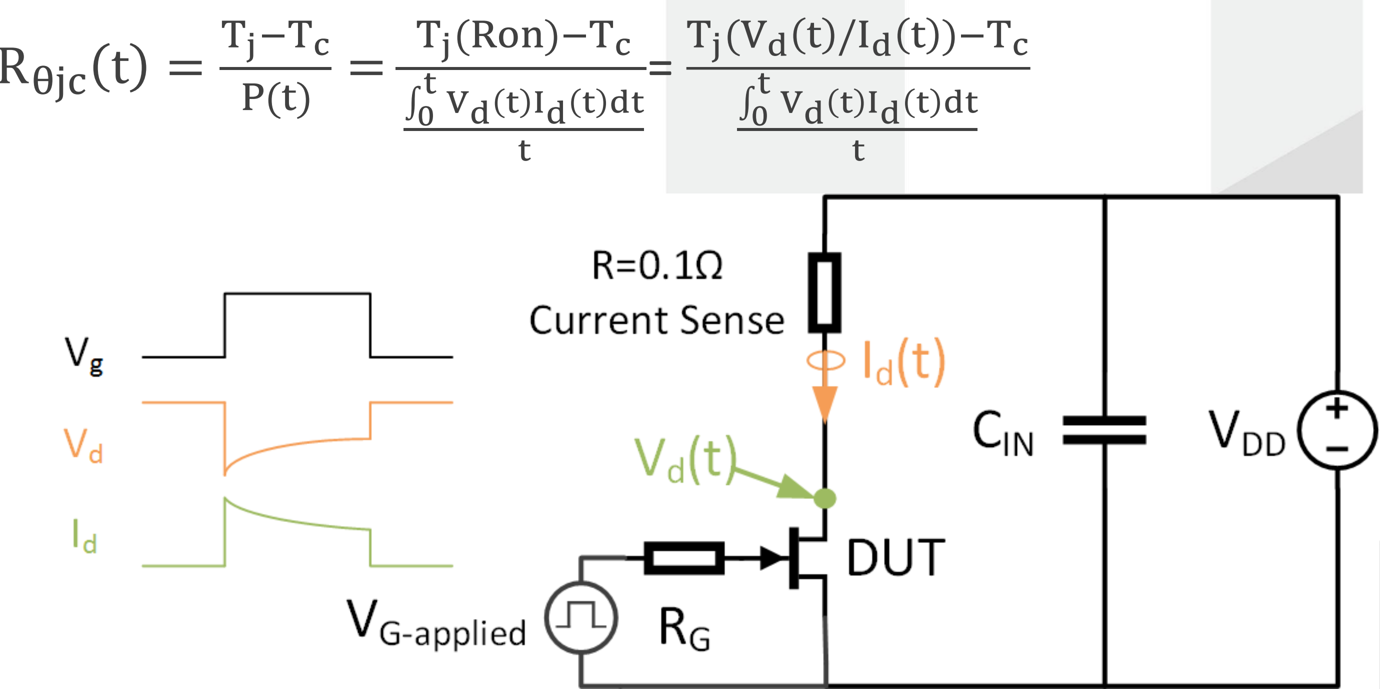
Technology has improved over the past two years, the dynamic R_{dson} is better now than 2 years ago

Source: Rui Li, Xinke Wu, Gang Xie, Kuang Sheng, Dynamic On-state Resistance Evaluation of GaN Devices under Hard and Soft Switching Conditions, APEC 2018

Parameter Testing: Thermal Resistance

- To test the thermal resistance, we need to know the accurate junction temperature within the packaged device. (We can test the junction temperature using thermal imager or thermal coupler, but it needs to teardown the case)
- For MOSFET with PN junctions, body diode forward voltage V_f is monitored for sensing the junction temperature. GaN has no body diode. Instead, R_{dson} is used to sense the $T_{j,}$, which means $T_j = T_j(R_{on})$

$$R_{\theta jc}(t) = \frac{T_j - T_c}{P(t)} = \frac{T_j(Ron) - T_c}{\frac{\int_0^t V_d(t) I_d(t) dt}{t}} = \frac{T_j(V_d(t)/I_d(t)) - T_c}{\frac{\int_0^t V_d(t) I_d(t) dt}{t}}$$



R_{thJC} from Various Packaging Forms

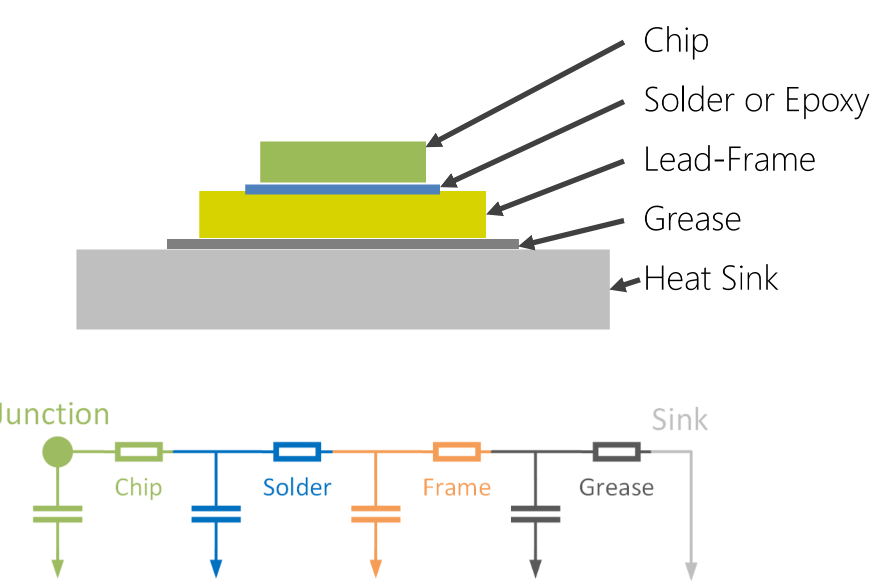
	Package Type	R_{dson}	Material	R_{thJC}
IPP65R065C7	TO220	65mΩ/33A	Si	0.73 K/W
IPL65R070C7	ThinPAK 8x8	70mΩ/28A	Si	0.74 K/W
IPW60R060P7	TO247	60mΩ/48A	Si	0.76 K/W
IPB65R065C7	TO263	65mΩ/33A	Si	0.73 K/W
IGLD60R070D1	DFN 8x8	70mΩ/15A	GaN	1.1 K/W

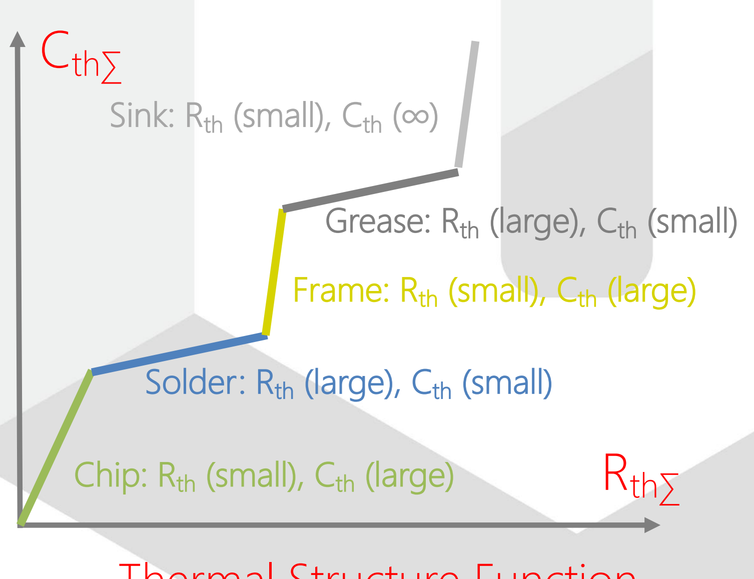
All data from Infineon datasheet

Parameter Testing: Thermal Impedance

- Thermal resistor determines how much power it will dissipate for certain temperature change, while thermal capacitor governs the thermal capacity, or how much heat it can hold on

- Sometimes in Failure Analysis, we use thermal impedance as a guideline for damage caused by either Temperature Cycling (TC) or Power Cycling (PoC). TC tests how the external temperature impact device life-time, while PoC tests how the self-heating gradually damage the device internally

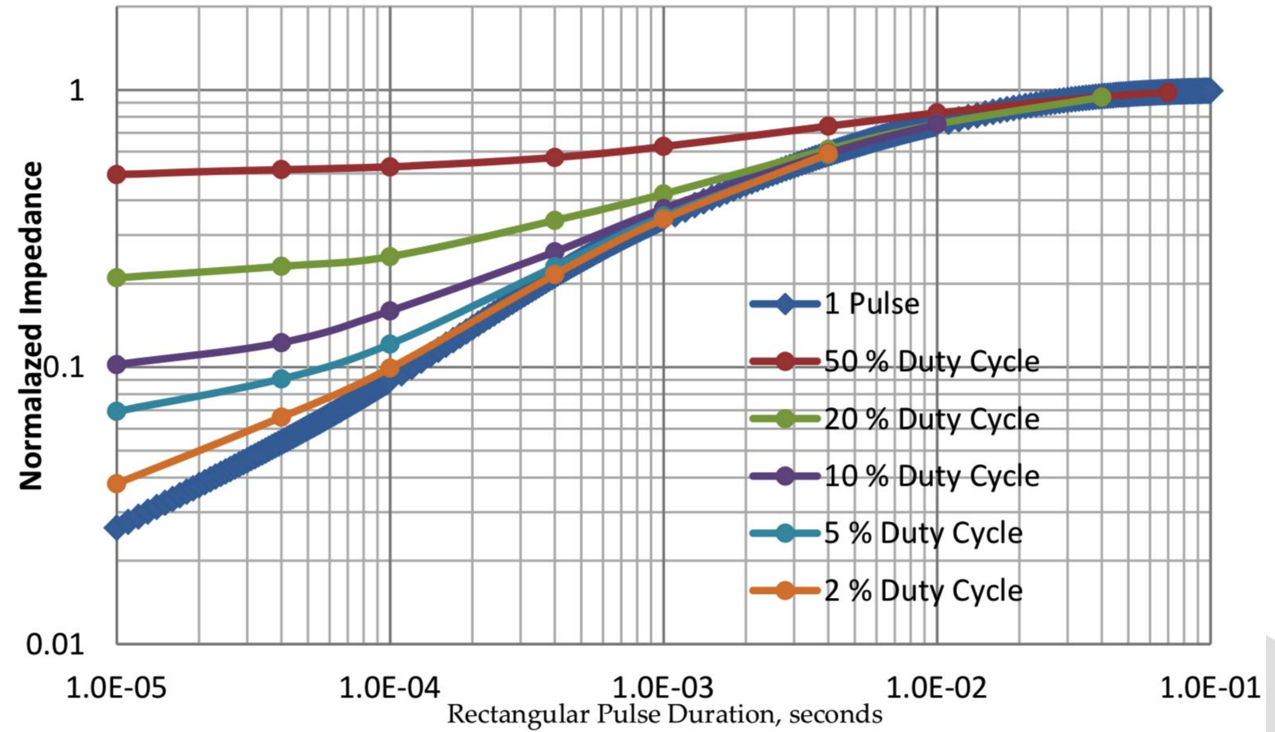




Thermal Structure Function

Parameter Testing: Transient Thermal Impedance

- DC thermal impedance is the maximum thermal impedance at steady state
- The transient thermal impedance is a measure of how the device behaves when pulsed power is applied to it. This is important for determining the behavior of low duty cycle, low frequency pulsed loads
- For the same power level, at short durations, the thermal impedance appears to be smaller



GaN systems: Transient thermal modeling of gallium nitride devices (http://tesint.com/docs/Transient_Thermal_Modeling_of_Electronic_Devices_Using_ElectroFlo.pdf)

How to Rate Continuous Current?

$$\frac{1}{2} I_{dsmax}^2 R_{dson@T_{Jmax}} = \frac{T_{Jmax} - T_c}{R_{thJC}}$$

$$I_{dsmax} = \sqrt{\frac{T_{Jmax} - T_c}{R_{dson@T_{Jmax}} R_{thJC}}}$$

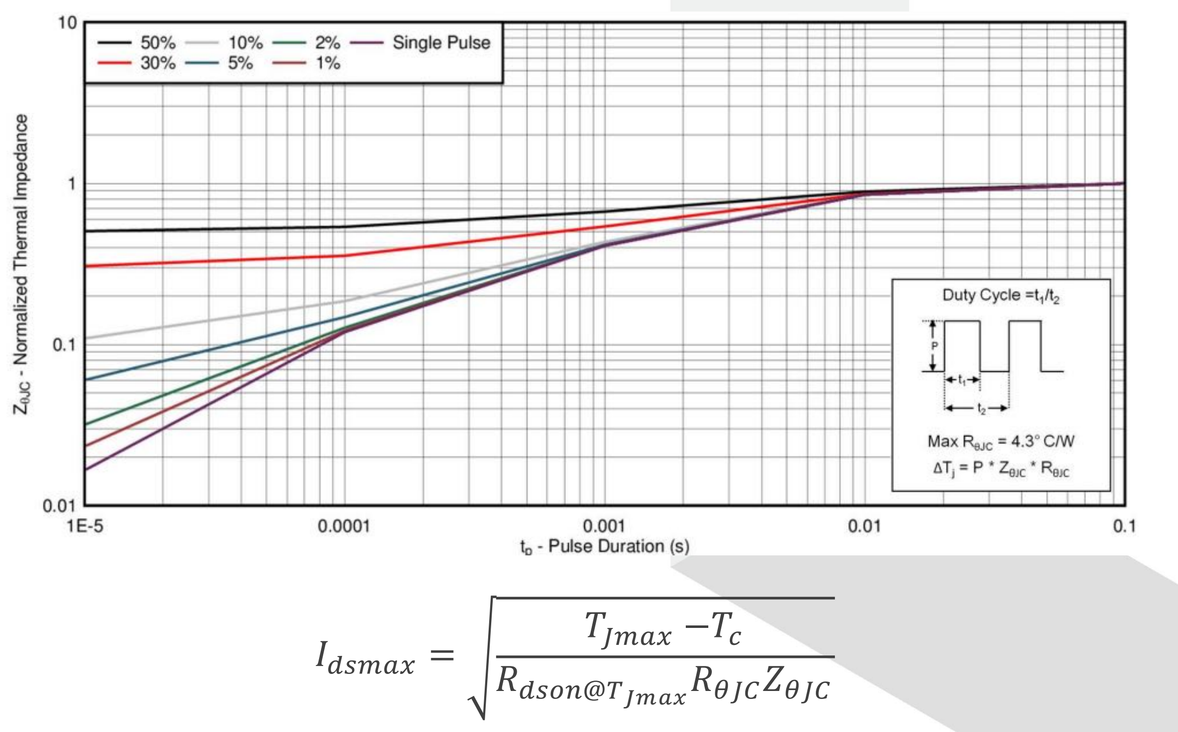
- I_{ds} calculated from this method reflects the upper current limit. To keep a safety margin, the current rating is usually lower than the calculated value
- As an example, for CoolMOS IPB65R095C7, $R_{dson@TJmax}$=0.202, R_{thJC}=0.98, I_{dsmax} from the above equation calculated as 25.13A. This device is rated as 24A by Infineon
- Another current limiting factor is bond wire fusing. But most of the time bonding wires fuse only when devices fail

Why GaN has a lower current rating with same R_{dson}?

- With the same packaging forms and similar R_{dson}, the continuous current of GaN is rated much lower than silicon, due to the fact that with the same R_{dson}, GaN chip size is usually much smaller than silicon counter part, which increases thermal resistance R_{thJC}
- As an example, for a GaN device with $R_{dson@TJmax}$=0.26Ω, R_{thJC}=1.0K/W, I_{dsmax} from the above equation calculated as 22A. This device is rated as 15A by the GaN manufacturer for some safety margins
- Also, the total area of lead-frame bonding pads determine how many bonding wires with certain thickness (1mil, 2mil?) can be applied. These bonding wires have limited current handling capabilities and can be the bottleneck for some packaging types (such as DFN)
- For GaN manufacturers such as GaNPower, we use the same chip in different packaging forms (such as TO220, DFN, etc...), the current ratings are always less meaningful than R_{dson} values

How to Rate Pulsed Current

- The rating of max pulsed current is similar to that of a continuous current in that both current ratings are calculated rather than tested.
- The pulsed current rating is based on the current pulse duration and duty cycle specified (e.g. 100us duration and duty cycle=1%), with regard to the transient thermal impedance

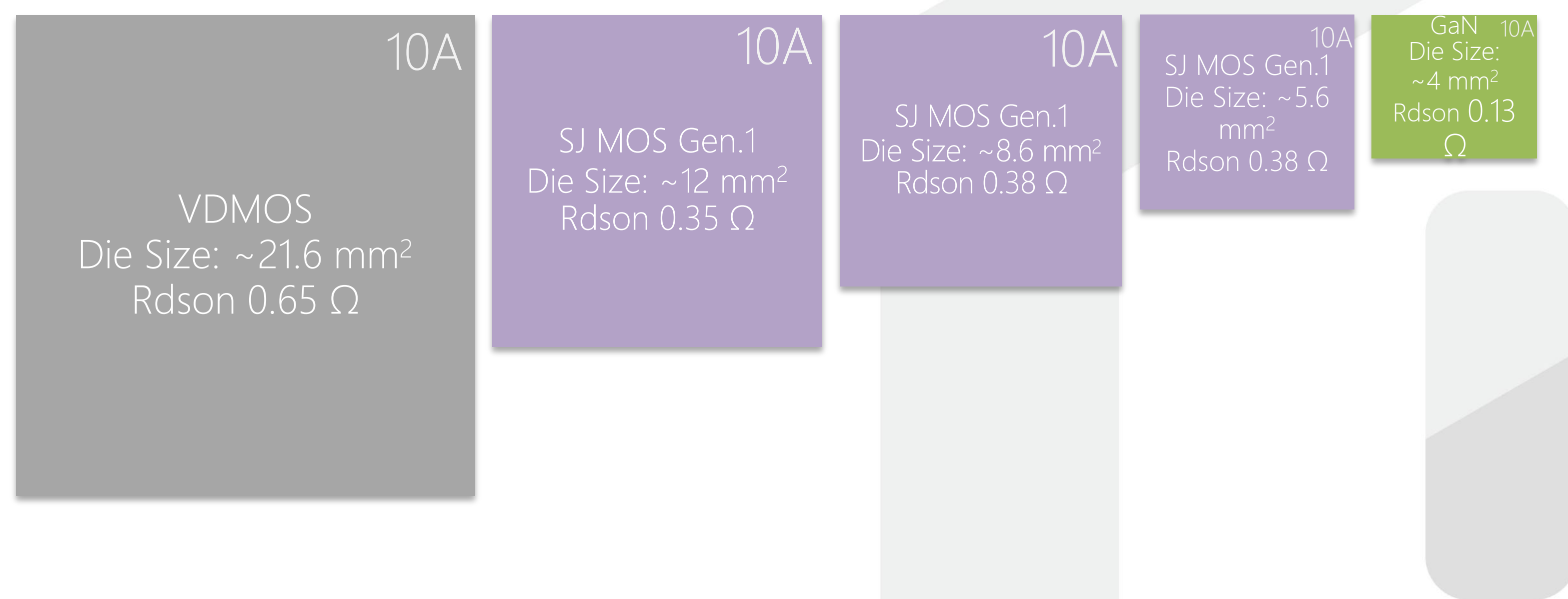


$$I_{dsmax} = \sqrt{\frac{T_{Jmax} - T_c}{R_{dson@T_{Jmax}} R_{\theta JC} Z_{\theta JC}}}$$

https://e2e.ti.com/blogs_/b/powerhouse/archive/2015/06/29/understanding-mosfet-data-sheets-part-4-mosfet-switching-times

© Fred Yue Fu (傅玥), GaNPower International Inc.

Chip Sizes Compared



- SJ Chip size shrinks during the past 20 years. However, GaN is a quantum leap, even with lateral structures.
- Smaller chip size means lower cost for the same technology

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FOM Comparison (SJ MOS vs. GaN)

FOM (R_{dson} · Q_g) (Ω · nC)

Device	FOM
SJ MOS Gen 1 (600V/0.19Ω)	16.5
SJ MOS Gen 2 (600V/0.19Ω)	12
SJ MOS Gen 2.5 (600V/0.19Ω)	6.4
SJ MOS Gen 3 (600V/0.18Ω)	4.3
GaN HEMT (650V/0.22Ω)	0.37

Parameter Testing: SOA

- GaN has similar SOA definition as Silicon devices
- The thermal instability region indicates where thermal runaway can occur, and the steeper the slope, the more prone the FET is to enter this thermal runaway condition at higher breakdown voltages
- TLP (Transmission Line Pulse) can be used to test the device SOA boundary

Current Limitation
$R_{DS(on)}$ Limitation
Max Power Limitation
Thermal Instability Limitation
BV_{DSS} Limitation
DC, 10 ms, 1 ms, 100 µs
I_{DS} - Drain-to-Source Current (A)
V_{DS} - Drain-to-Source Voltage (V)

SOA - Measured Points
I_D (A)
V_{DS} (V)
100us, 1ms, 10ms, 100ms

TPH3208PS
Calculated SOA
10μs, 100μs, 1ms, 10ms
Ids [A]
Vds [V]

TP65H035WSQA
Measured SOA
1μs, 10μs, 100μs, 1ms, 10ms
Ids [A]
Vds [V]

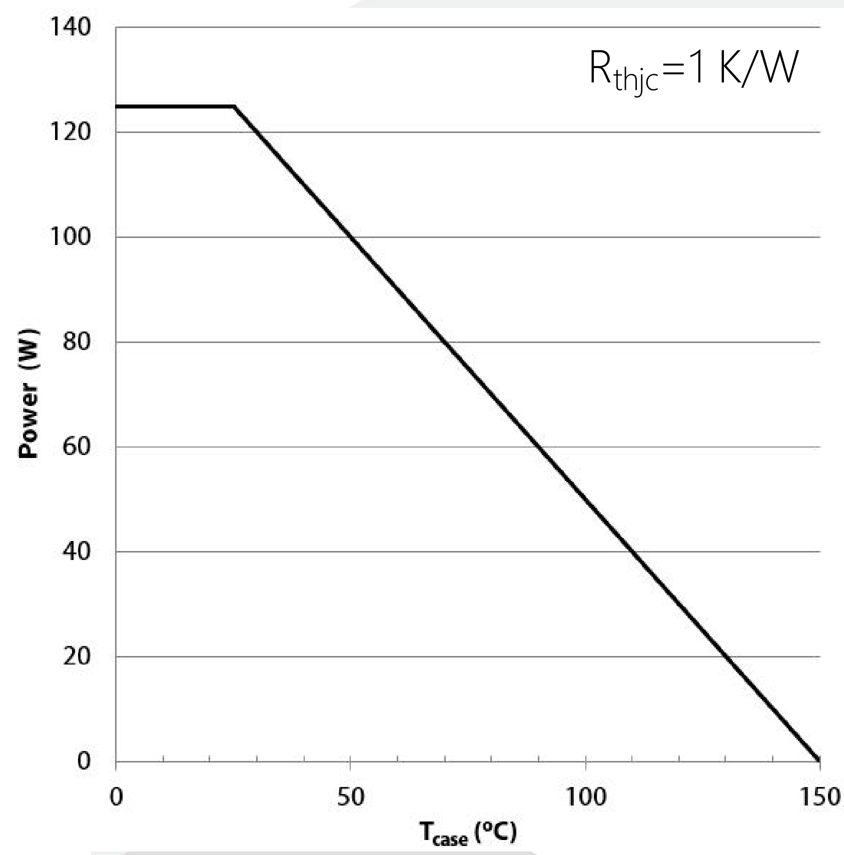
https://e2e.ti.com/blogs_/b/powerhouse/archive/2015/05/02/understanding-mosfet-data-sheets-part-2-safe-operating-area-soa-graph Datasheet www.transphormusa.com

Parameter Testing: Power Ratings

- With R_{thJC} available, we can use this equation to calculate the max power allowed:

$$P_{max} = \frac{T_{Jmax} - T_c}{R_{thJC}}$$

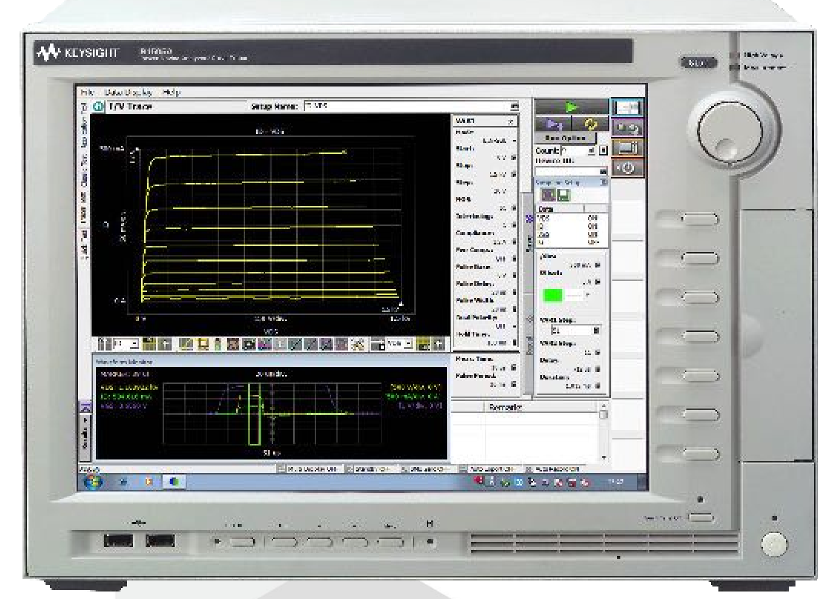
- A power vs. case temperature curve can then be drawn based on the equation above



Reference: GaN Systems Datasheet

Datasheet Testing: Keysight B1505A/B1506A

- Keysight 1500 series is a one stop power device parameter testing platform, with All-in-one solution for power device characterization up to 1500A/10kV
  - ✓ Fully automated Capacitance (C_{iss}, C_{oss}, C_{rss}, etc.) measurement at up to 3000V of DC bias
  - ✓ Gate charge measurement
  - ✓ High voltage/high current fast switch option to characterize GaN current collapse effect
  - ✓ Perform both hot and cold temperature dependency testing in an interlock equipped test fixture



Source: https://www.keysight.com/

Double Pulse Tests: Methods

- The load inductor is used to establish the desired current during the first pulse and keep this current nearly constant during the subsequent turn-off and turn-on transients.
- The capacitors are employed to maintain a stable DC bus voltage. Bulk capacitors with large capacitance supplies energy to establish the inductive current during the first pulse, while the decoupling capacitor with low parasitic equivalent series inductance (ESL) is responsible for supplying transient current during the switching transition.
- A bleeder resistor is introduced across the DC bus to dissipate the remaining energy stored at the DC capacitors
- The DPT signals are generated either by a signal generator or by a MCU

DC
Bleeder Resistor
R1
C1
Energy Storage Capacitor
Decoupling Capacitor
C2
Double Pulse Gate Drive
Q2
L1
Q1
GaN DUT

V_{GS}
V_{DS}
I_{DS}

Source: Fei (Fred) Wang, Zheyu Zhang, and Edward A. Jones, Characterization of Wide Bandgap Power Semiconductor Devices; published by The Institution of Engineering and Technology 2018

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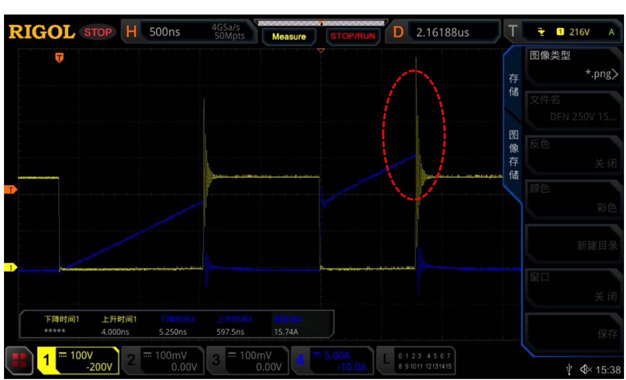
Double Pulse Tests: Descriptions

- With a constant voltage and a given inductor in the test, there is a constant current change rate di/dt during turn-on.
- The width of the first pulse is set to achieve the current you want to observe, for device characterization this often is the device's rated current.
- At the end of the first pulse, the double pulse test allows to observe "turn-off rated current".
- The current commutates to the freewheeling diode and gets back to the GaN when turning on the second pulse. An oscilloscope properly set will observe "turn-on of rated current" at the rising edge of the second pulse. However, during the turn-on period, the current in the device grows and does so exceeding the rated current. As everything you want to learn takes place during the rising edge, the second pulse can be as short as possible.
- The important parts are the falling edge of pulse one and the rising edge of pulse two.

http://athenaenergycorp.com/wp-content/uploads/2016/03/Rogowski_doublepulse_testing.pdf

Double Pulse Tests: Some Tips

- In DPT, it is important to have a low inductance loop to minimize the V_{ds} voltage overshoot.
- For current measurement, a current probe requires additional wiring, which brings high frequency inductance. It is necessary to insert a dynamic current measurement, typically coaxial shunt, into the switching loop.
- Gate loop is not from the gate drive IC to the device, but from the gate drive decoupling capacitor to gate drive IC and then the device. Magnetic field cancellation concept can be used to minimize the gate loop parasitics.



Double pulse test with additional wiring for current probing

Double pulse test without additional wiring for current probe

A typical coaxial shunt for current sensing

Contents

- Session 1: GaN devices basics
  - GaN, An Introduction
  - GaN Design, Fabrication and Testing
  - GaN Compact Modeling and Reliability
- Session 2: GaN Gate Driving
- Session 3: GaN Applications

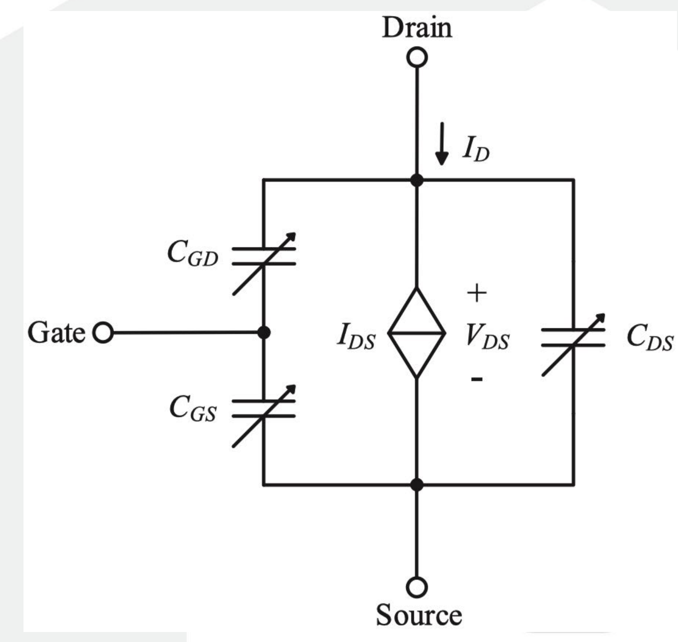
Compact Modeling of GaN HEMT

- There are three compact modeling methods: physics-based, semiphysics-based or behavioral model

- The physics-based model is based on the physical structure and internal parameters of GaN HEMT, which is very accurate, however, it's not suitable for power electronics circuit simulations due to the complicated physical parameter extraction process, as well as the long simulation time

- Semiphysics-based model is partly based on the physical structure and internal parameters of GaN HEMT, and some behavioral equations are included

- Behavioral model is mainly based on behavioral equations of GaN HEMT, the information about the physical structure and the internal parameters of GaN HEMT is not necessary any more



Hong Li, Xingran Zhao, Wenzhe Su, Kai Sun, Trillion Q. Zheng and Xiaojie You; Non-segmented PSpice Circuit Model of GaN HEMT with Simulation Convergence Consideration, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS 2017

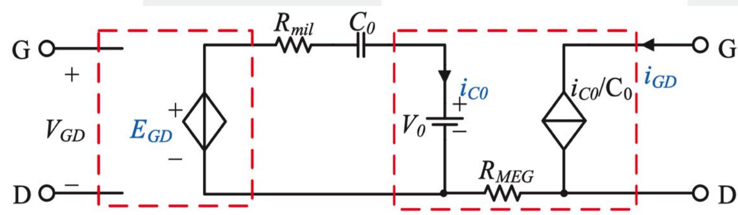
Compact Modeling of GaN HEMT: Behavioral model Example

- For static modeling that takes temperature into account:

$$
\begin{cases}
I_{DS} = K_1(T)\cdot \ln[1+\exp\left(\dfrac{V_{GS}-b_1}{c_1}\right)] \cdot \dfrac{(m_1+n_1\cdot V_{GS})V_{DS}}{1+P_1(T)\cdot(d_1+e_1\cdot V_{GS})V_{DS}}, & V_{DS}>0 \\
I_{DS} = \text{-}K_2(T)\cdot \ln[1+\exp\left(\dfrac{V_{GD}-b_2}{c_2}\right)] \cdot \dfrac{V_{SD}}{1+P_1(T)\cdot V_{SD}}, & V_{DS}\le 0
\end{cases}
$$

$$
\begin{cases}
K_1(T) = K_1\cdot[1-l_1\cdot(T-25)] \\
K_2(T) = K_2\cdot[1-l_2\cdot(T-25)] \\
P_1(T) = [1-h_1\cdot(T-25)] \\
P_2(T) = [1-h_2\cdot(T-25)]
\end{cases}
$$

- For dynamic modeling that takes temperature into account:



$$
\begin{cases}
i_{GD} = s\cdot \dfrac{1}{1+\exp\left(\dfrac{p-V_{GD}}{q}\right)} + r \\
E_{GD} = s\cdot q\cdot \ln[1+\exp\left(\dfrac{V_{GD}\text{-}p}{q}\right)] + r\cdot V_{GD}
\end{cases}
$$

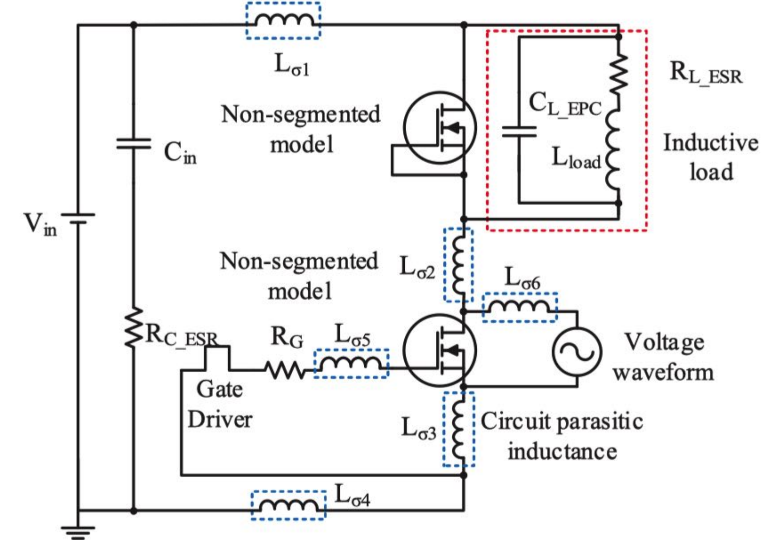
- Model parameters are extracted with measurement data

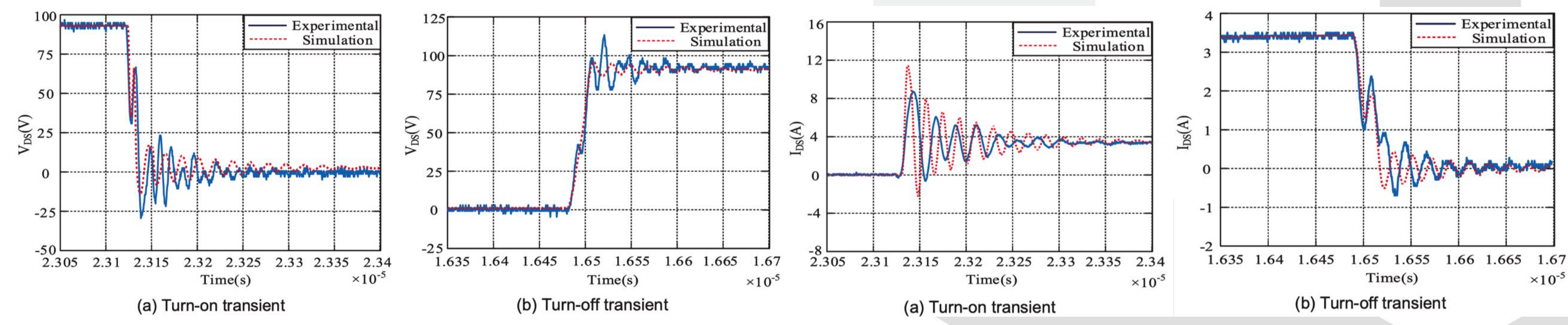
Hong Li, Xingran Zhao, Wenzhe Su, Kai Sun, Trillion Q. Zheng and Xiaojie You; Non-segmented PSpice Circuit Model of GaN HEMT with Simulation Convergence Consideration, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS 2017

Compact Modeling of GaN HEMT: Behavioral model Example

- In order to have an accurate simulation, all the parasitics in the circuitry should be included. The numbers can be extracted from either measurements or 3D structural simulations such as Ansoft Q3D:

- Good fits can be obtained from proper parameter extraction for the behavior compact model:



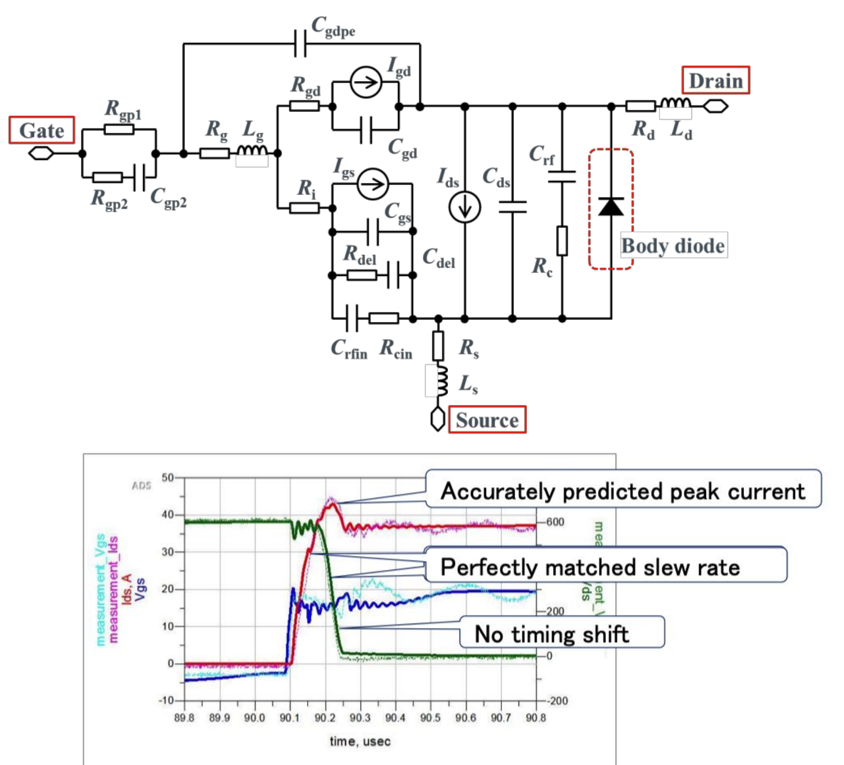


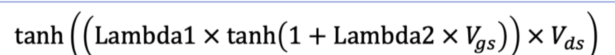
(a) Turn-on transient (b) Turn-off transient (a) Turn-on transient (b) Turn-off transient

Hong Li, Xingran Zhao, Wenzhe Su, Kai Sun, Trillion Q. Zheng and Xiaojie You; Non-segmented PSpice Circuit Model of GaN HEMT with Simulation Convergence Consideration, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS 2017

Compact Modeling of GaN HEMT: Behavioral model Example

- Similar modeling method (behavioral model) is also provided by Keysight technologies:
  - Measured device characteristics turned into mathematical representation
  - Accurately represents device behavior which can't be achieved with any physics-based model
  - Less parameters with better conversion
  - Independent of device physics parameters (e.g. T_{ox}) → Everyone (e.g. circuit designer) can use





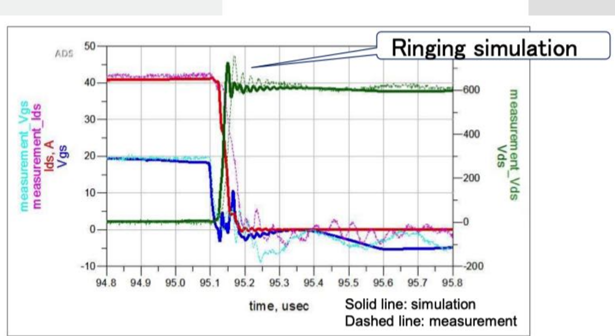
$$\tanh\left(\left(\mathrm{Lambda1} \times \tanh\left(1 + \mathrm{Lambda2} \times V_{gs}\right)\right) \times V_{ds}\right)$$

Added Vgs, Vds dependent parameter to drain current equation to better represent unsaturated drain current

$$Q_{gs} = \left(C_{gspi} + C_{gs0} \times \tanh 02\right) + \left(C_{gspi} + \left(C_{gs0} \times \tanh 01 + C_{gs0i} \times \tanh 1i\right) \times \tanh 02\right)$$

$$\tanh XX(i) = 1 + \tanh\left(A + B \times V_{gs} + C \times V_{ds}\right)$$

Added tanhXX to express a positive bias dependence on charge equation



APEC 2018: WBG power circuit simulation with extensive device characterization and modeling Keysight Technologies

Reliability Testing: Bathtub Curve

INFANT MOTALITY

(DECREASING FAILURE RATE)

JEDEC

USEFUL LIFE

(RAMDOM FAILURES)

JEDEC

WEAR OUT

(BEYOND PRODUCT LIEFTIME)

Reliability Testing: Examples

A typical JEDEC standard reliability tests for power devices should cover a long list of items, here is a highly simplified version to show some of the tested items

Test Items	Description	Requirements	Number of Chips from 3 lots each
HTGB	High Temperature Gate Bias	168h	77
HTRB	High Temperature Reverse Bias	168h	77
Temp. Cycles	Temperature Cycling Tests	-65°C / +150°C, 500 cycles, dwell time: 10-15minutes	77
PCT	Pressure Cooker Test	96h,T=121°C；RH=100%	77
THB	Temperature, Humidity, Bias Tests	1000h with bias	77
HTS	High Temperature Storage	150°C，1000hrs	77

Reliability Testing: JC-70

A new JEDEC committee: JC-70 was established in 2017 to deal specifically for wide band gap devices reliability issues. A sample proposed items for guidelines is listed below

REL

- List of Failure Mechanisms & Resulting Failure Mode
- Focusing on Charge Trapping, Charge Injection, Hot Electron, Corrosion, TDDB Like Mechanism, Delam
- Corresponding Acceleration & Stress Procedure

Test

- Dynamic R_{DS}(ON)
- Thermal Resistance (only for cascodes)
- Safe Operating Area (SOA)

Datasheet

- Include effect of Dynamic R_{DS}(ON)
- Nomenclature of parameters to adjust for uniqueness of GaN power transistors
- Transistor circuit symbol to reflect distinctive operation GaN HEMTs

Update: JEP173: Dynamic On-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices was released in 2019

Status of wide bandgap device qualification standards effort by new JEDEC committee JC70, APEC 2018

ISO , RoHS and IATF16949

Chemical Laboratory - Kao., SGS Taiwan Ltd.

Test Report No. : KA/2018/A0678 Date : 2018/10/16 Page : 1 of 14

SUMITOMO BAKELITE (TAIWAN) CO., LTD.
NO. 1, HWA SYI RD., TA FA INDUSTRIAL DISTRICT, TA LIAO, KAOHSIUNG, TAIWAN

The following sample(s) was/were submitted and identified by/on behalf of the applicant as :

Sample Description	:	EPOXY MOLDING COMPOUND
Style/Item No.	:	EME-G700H TYPE A SERIES (LOT NUMBER:8073202)
Sample Receiving Date	:	2018/10/09
Testing Period	:	2018/10/09 TO 2018/10/16
Sample Submitted By	:	SUMITOMO BAKELITE (TAIWAN) CO., LTD.

==

Test Requested :

(1) As specified by client, with reference to RoHS 2011/65/EU Annex II and amending Directive (EU) 2015/863 to determine Cadmium, Lead, Mercury, Cr(VI), PBBs, PBDEs, DBP, BBP, DEHP, DIBP contents in the submitted sample.

(2) Please refer to next pages for the other item(s).

Test Result(s) : Please refer to next page(s).

Conclusion :

(1) Based on the performed tests on submitted samples, the test results of Cadmium, Lead, Mercury, Cr(VI), PBBs, PBDEs, DBP, BBP, DEHP, DIBP comply with the limits as set by RoHS and amending Directive (EU) 2015/863.

Ray Chang Ph.D. / Manager - Tech
Signed for and on behalf of
SGS Taiwan Limited

An example of RoHS test certificate

- ISO is the basic requirement for semiconductor manufactures and packaging houses.
- RoHS (Restriction of Hazardous Substances) is generally required.
- IATF16949 is one of the automotive industry's most widely used international standards for quality management
- For fabless design house such as GaNPower, we rely on our foundry and packaging partners for these certificates

THANKS FOR WATCHING!

Contact us （Vancouver Headquarters）:

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