GaN Power HEMT Tutorial:
GaN Driving

GANPOWER INTERNATIONAL INC

Fred Yue Fu （傅玥）
Co-founder and COO
GaNPower International Inc.

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- Session 2: GaN Gate Driving
  - Gate driving basics
  - High dv/dt and di/dt issues
  - Gate drivers and isolation
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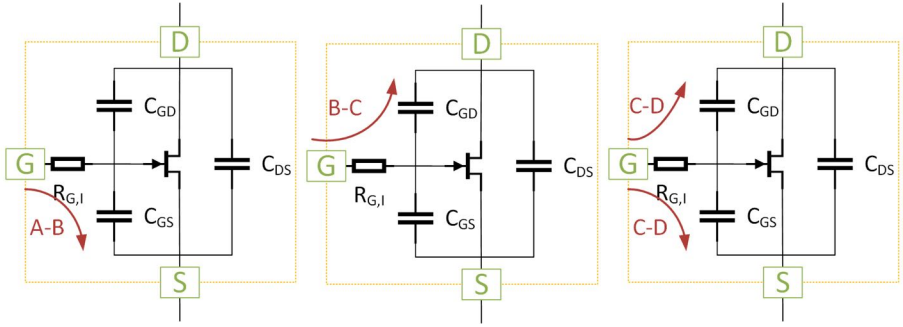
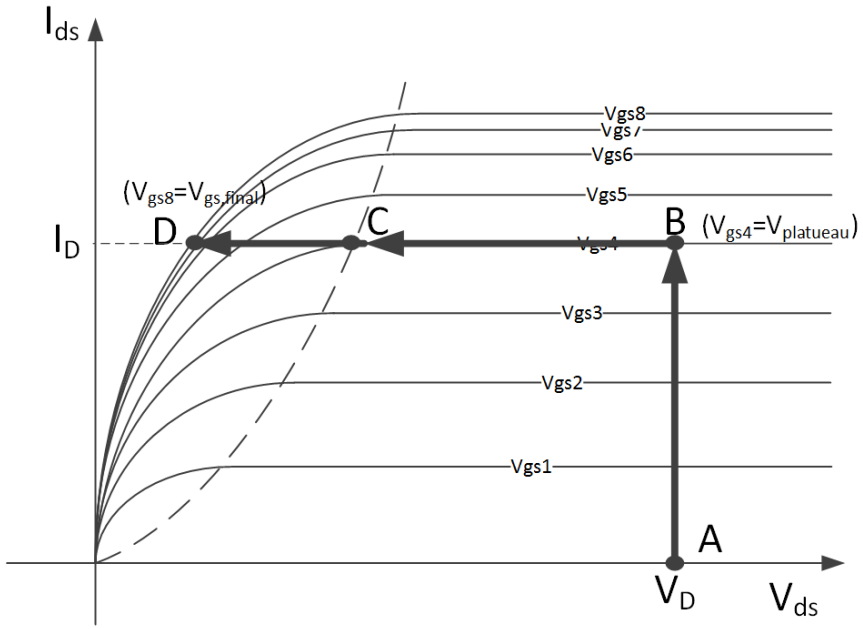
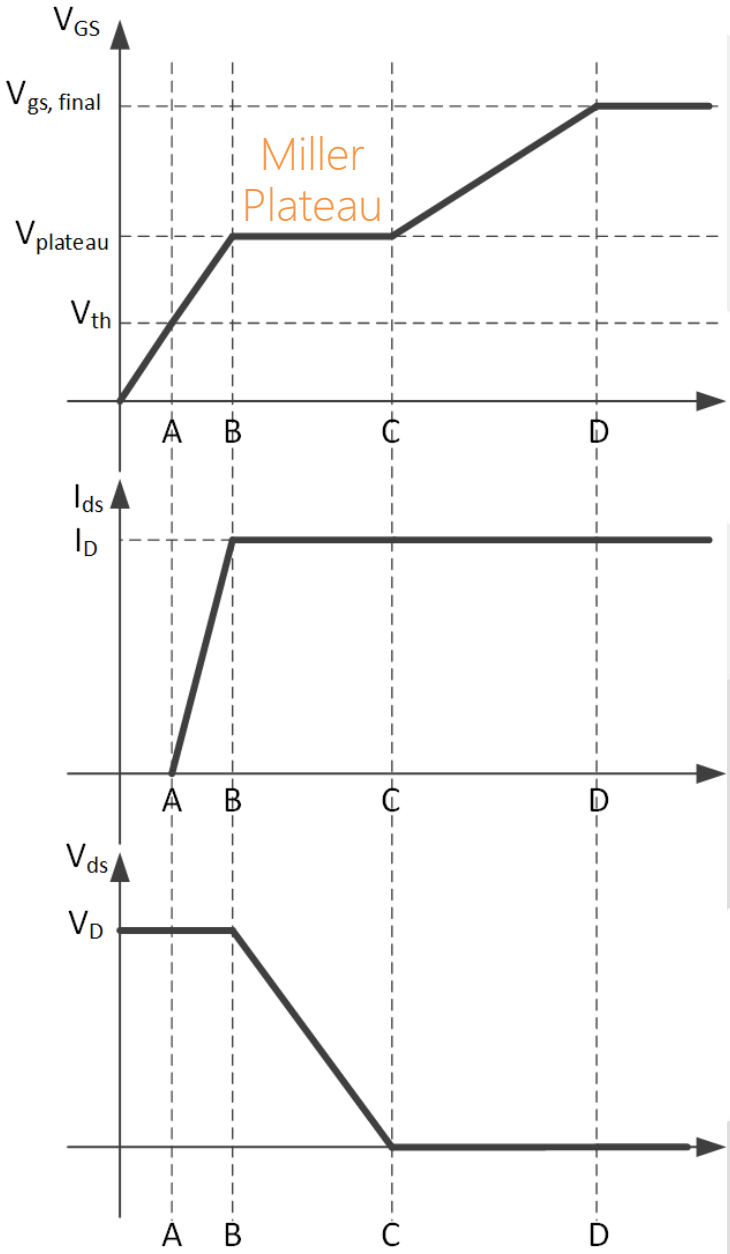
  - Co-package and monolithic GaN IC
- Session 3: GaN Applications

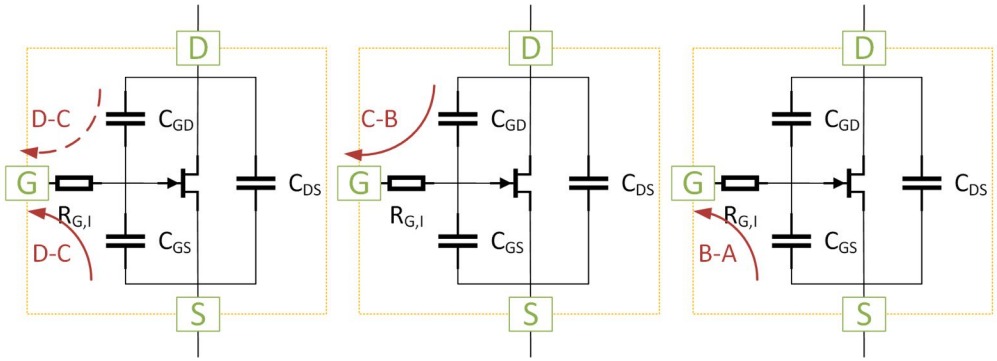
Gate Driving: Turn-on

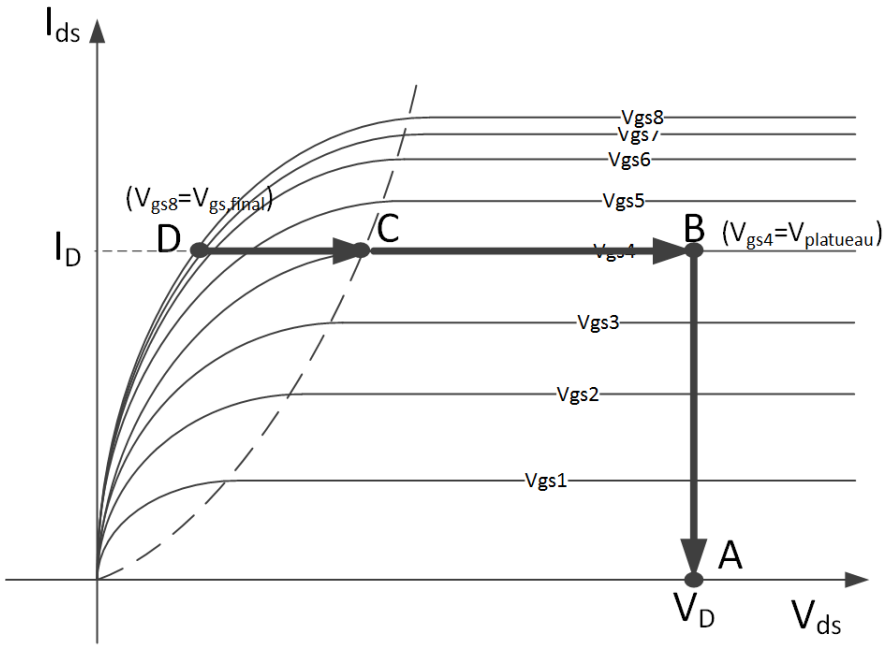


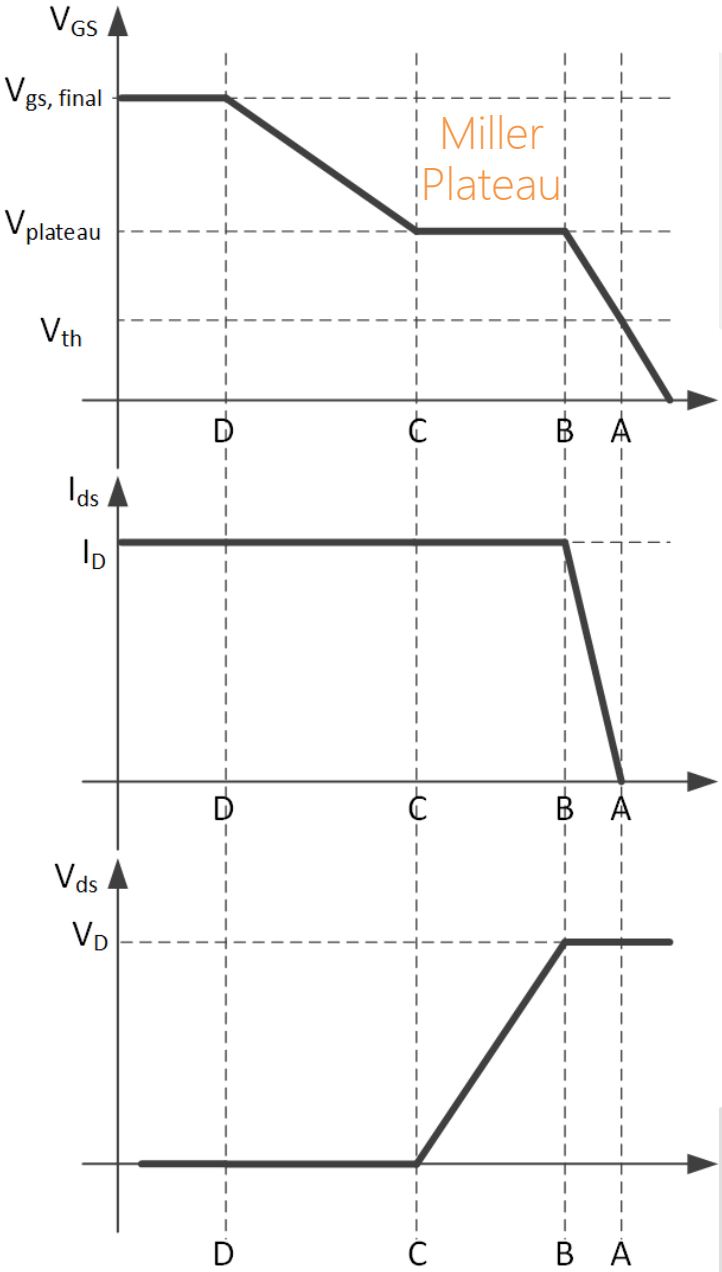




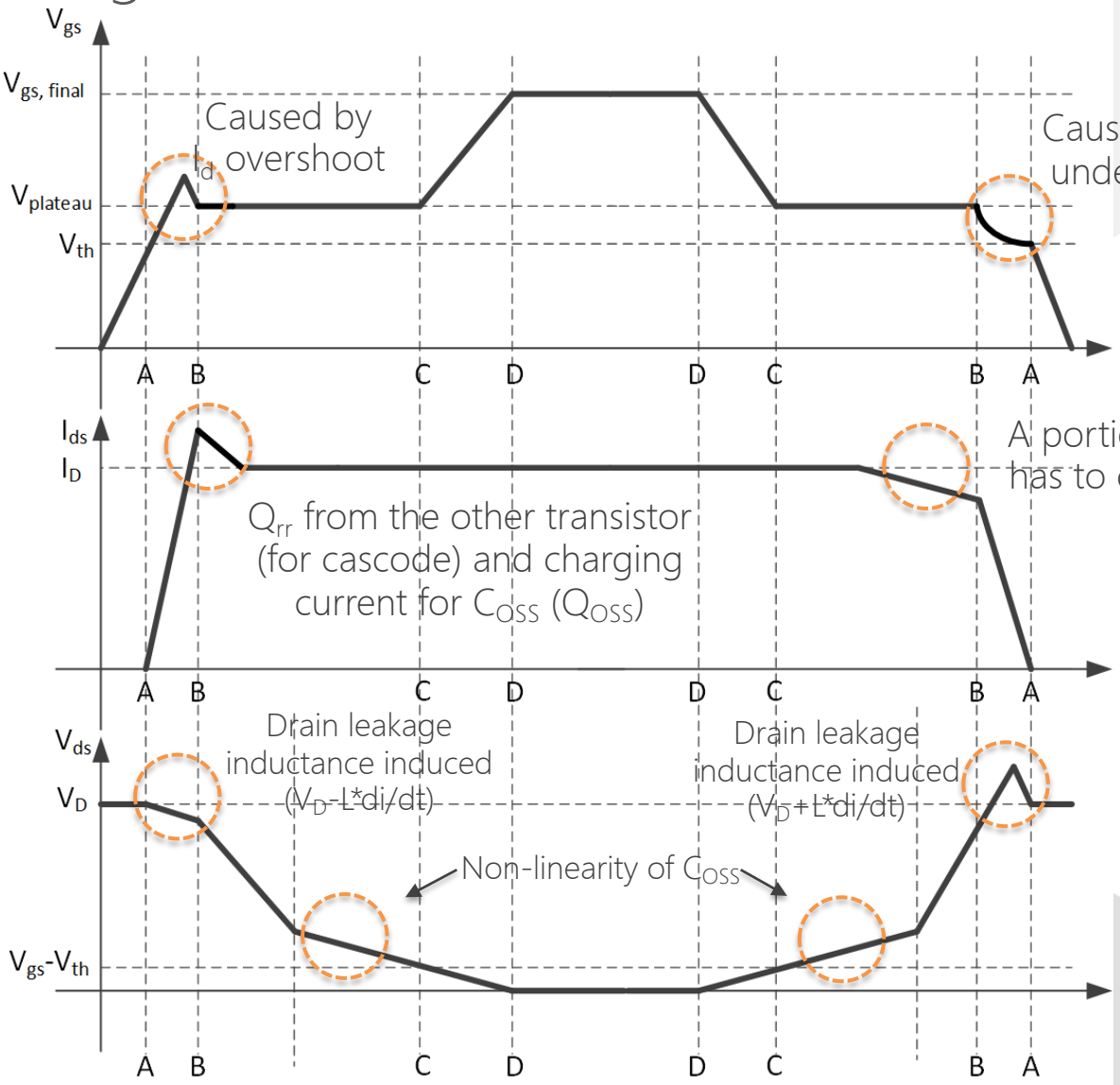
Gate Driving: Turn-off



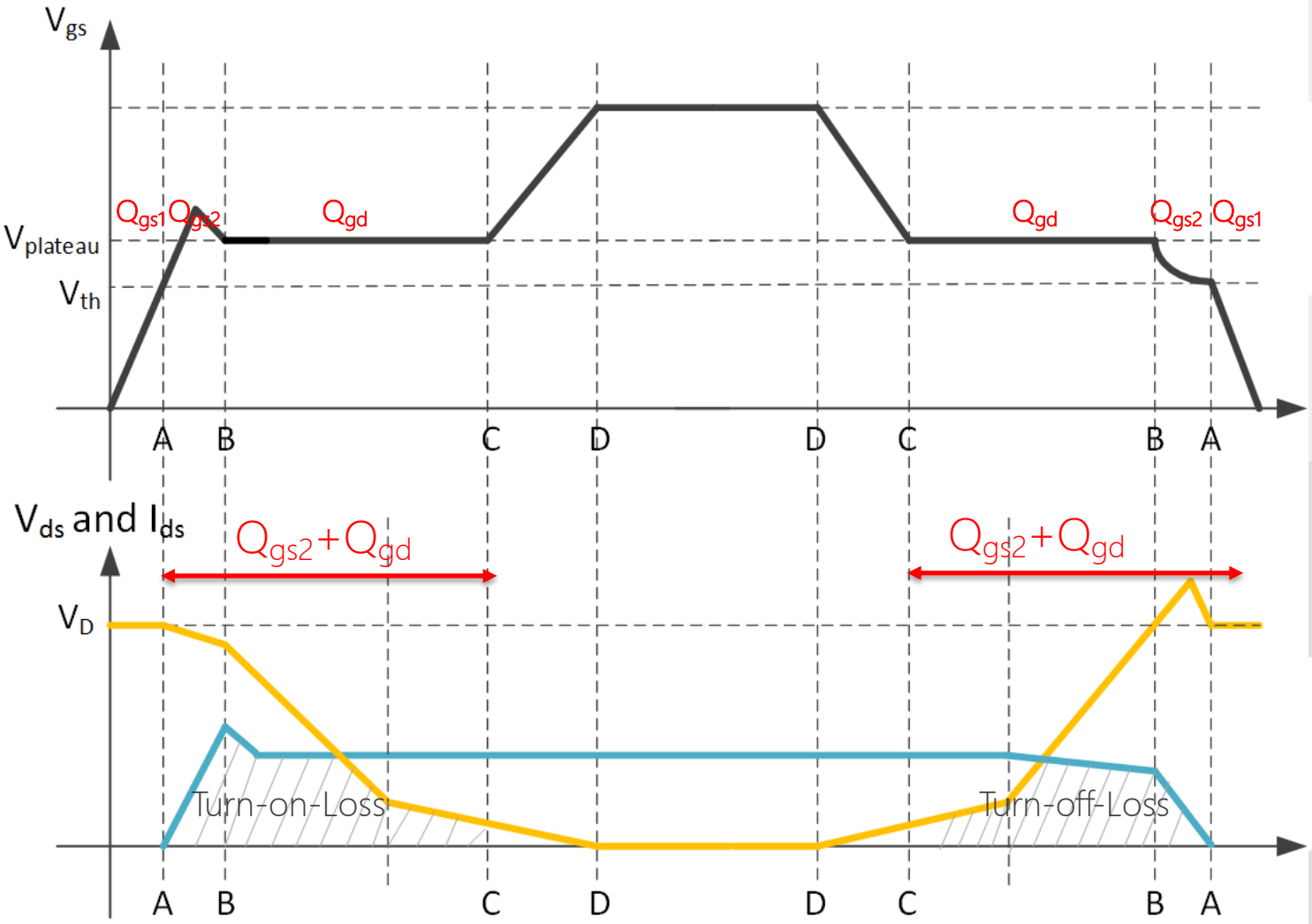




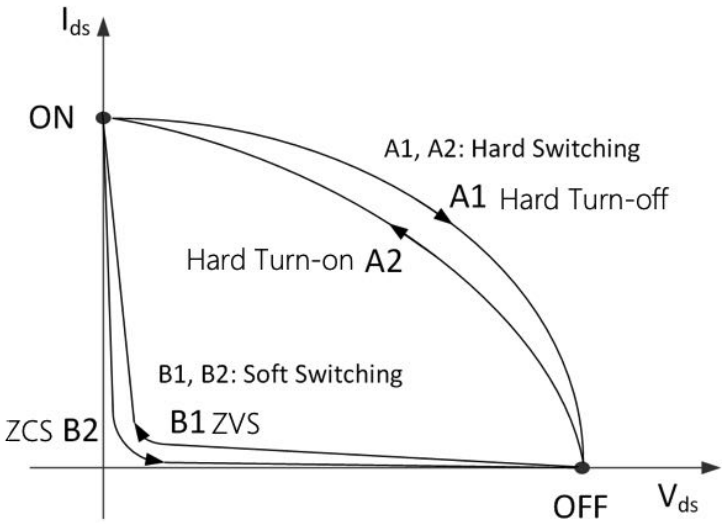
Gate Driving: Non-ideal case

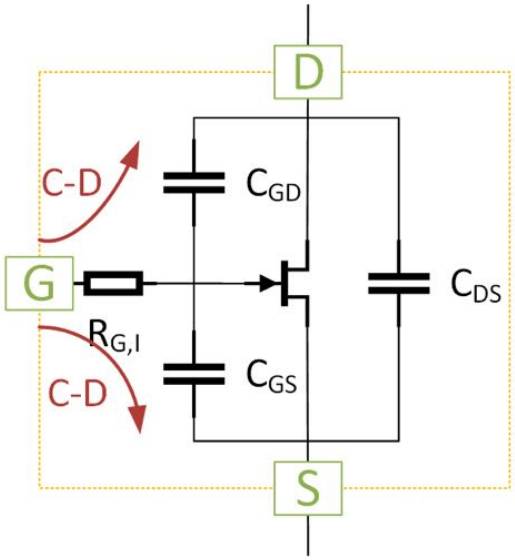


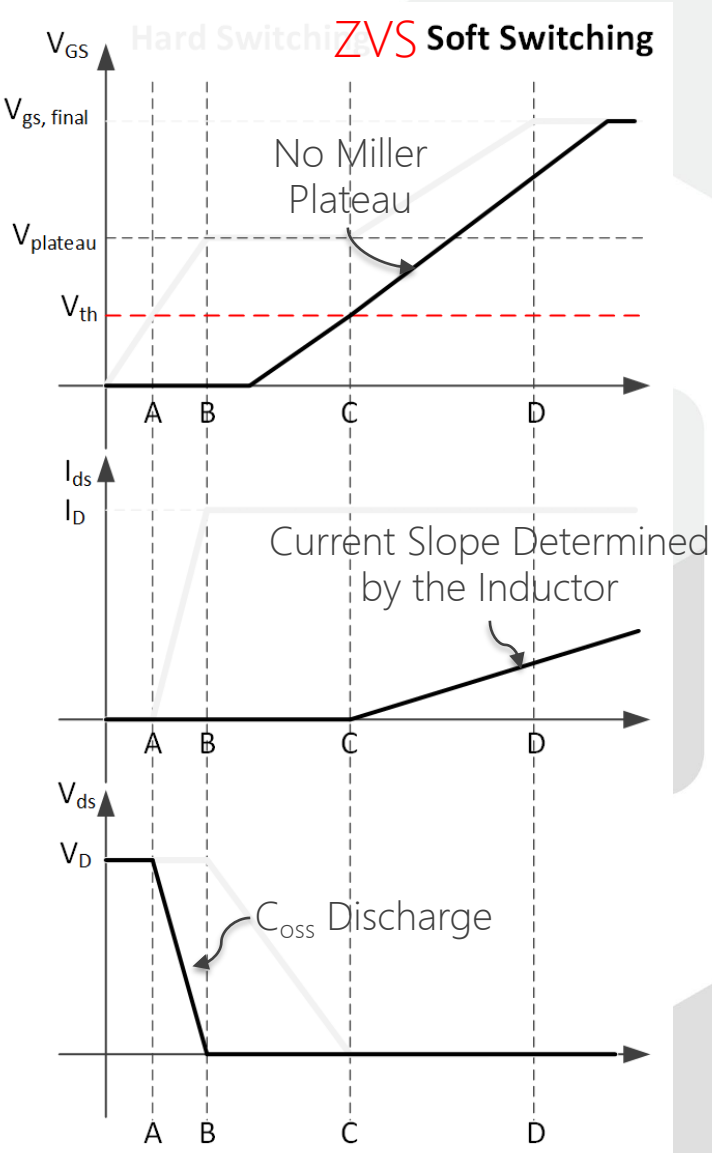
Gate Driving: Switching Loss



Gate Driving: Soft and Hard-switching Turning-on

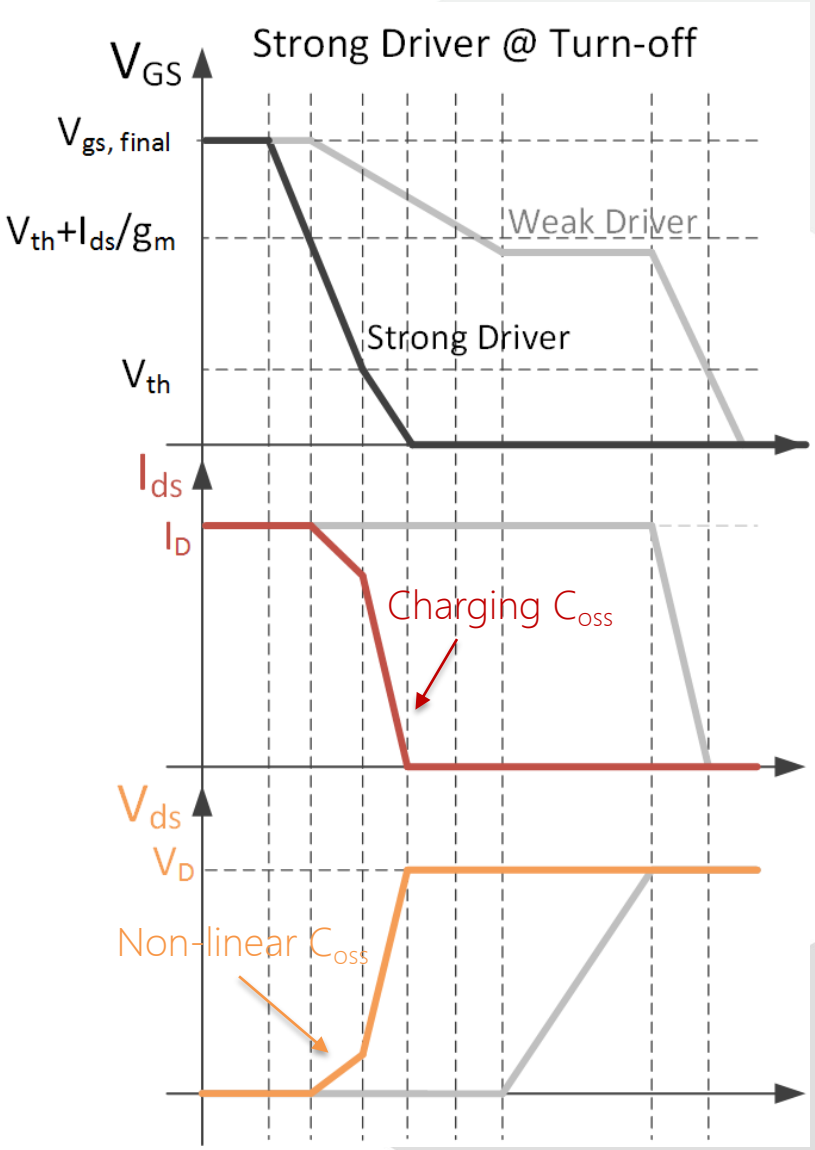






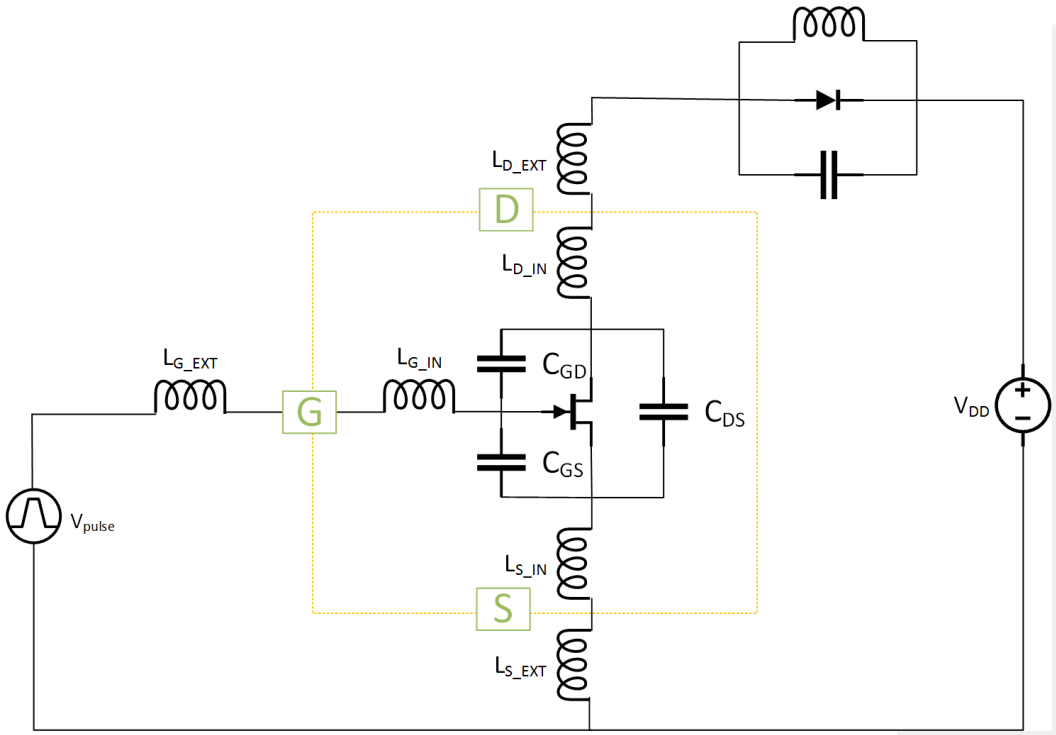
Gate Driving: Turning-off with Strong Driver

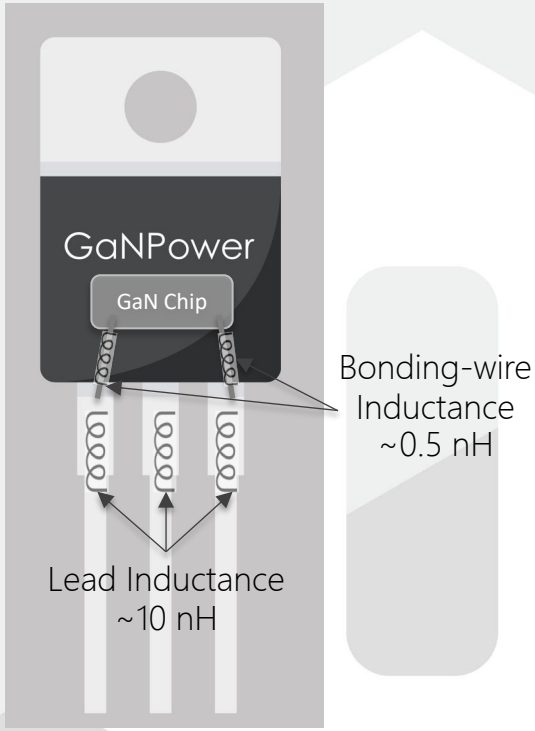
- ZVS provides soft-switching at turning-on, but turning-off is still hard switching
- A strong driver increases switching speed, reduces switching time and switching losses
- For a strong driver turn-off, Miller plateau may not be observed. This is exactly what we have seen when switching GaN devices off



Ref: Wei Zhang, Mastering the art and fundamentals of high voltage gate driver; TI High Volt Interactive

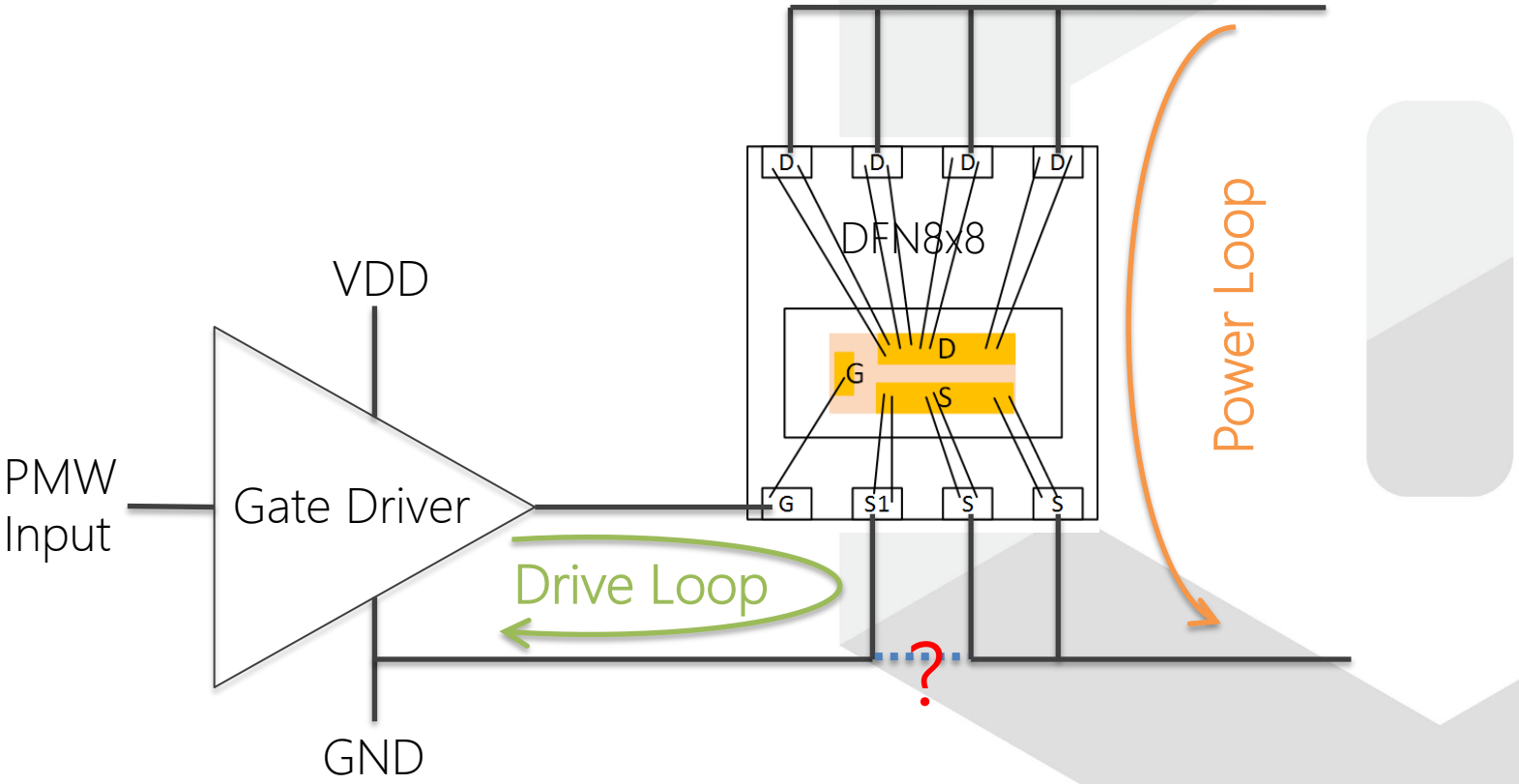
Gate Driving: Parasitic Inductance





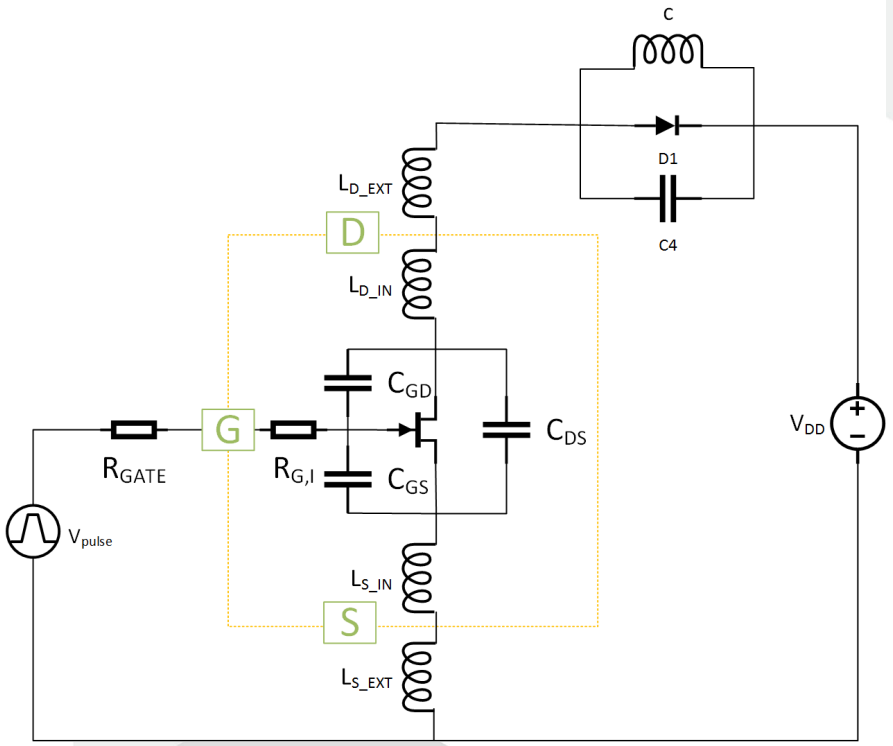
Gate Driving: Kelvin Source

Some device packaging types, such as DFN, have kelvin source pins, properly connecting the kelvin source to the drive loop will minimize the common source inductance (CSI)



Gate Driving: Parameters that affect switching loss

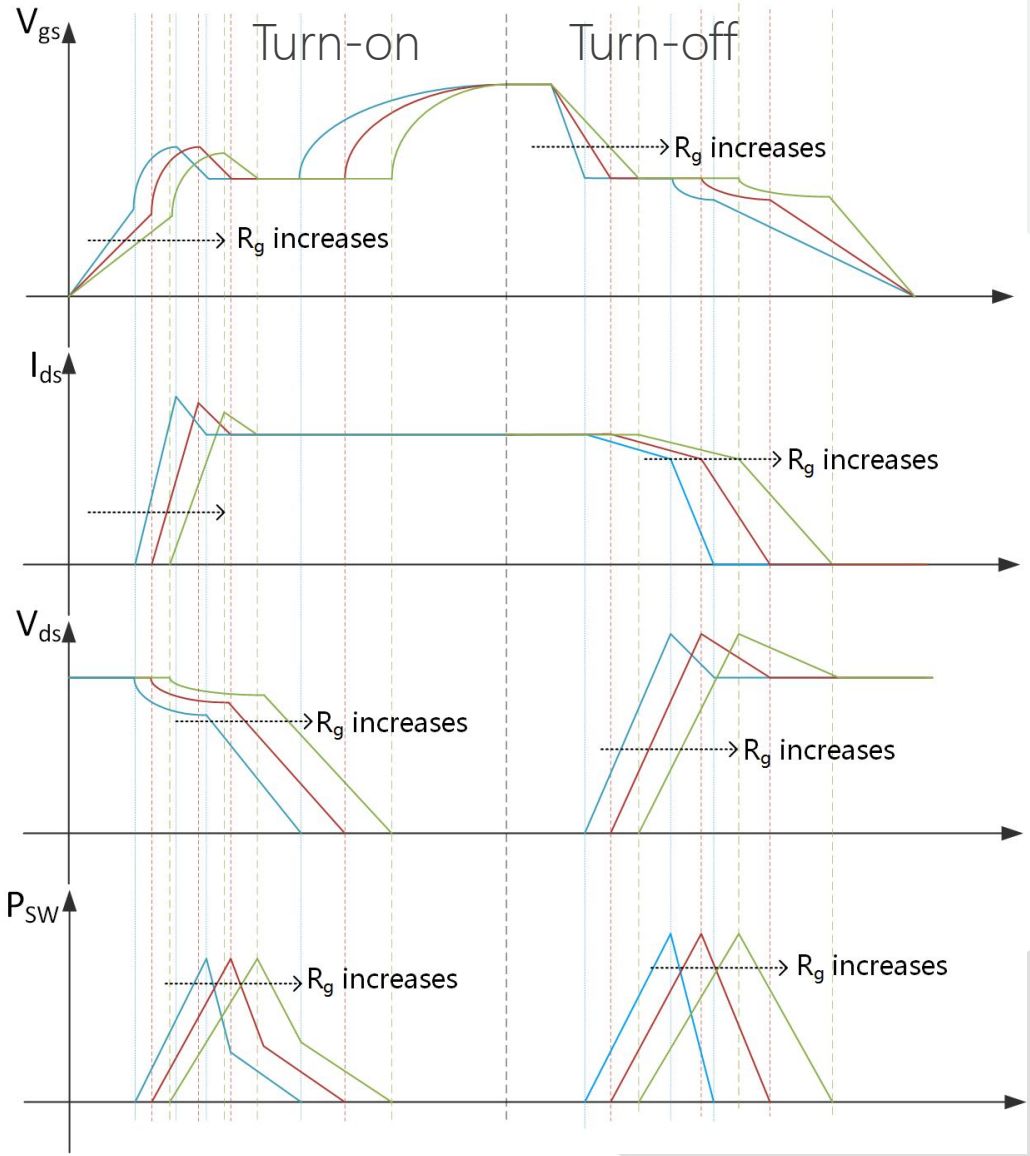
- Gate resistance R_g
- Gate to source capacitance C_{GS}
- Gate to drain capacitance C_{GD}
- Drain to source capacitance C_{DS}
- ....



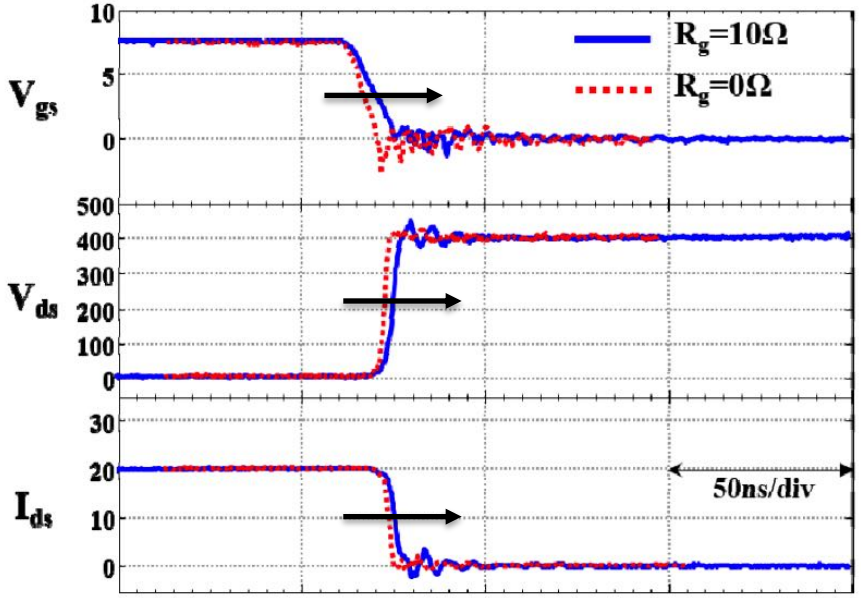
Gate Driving: R_g

R_g↑:

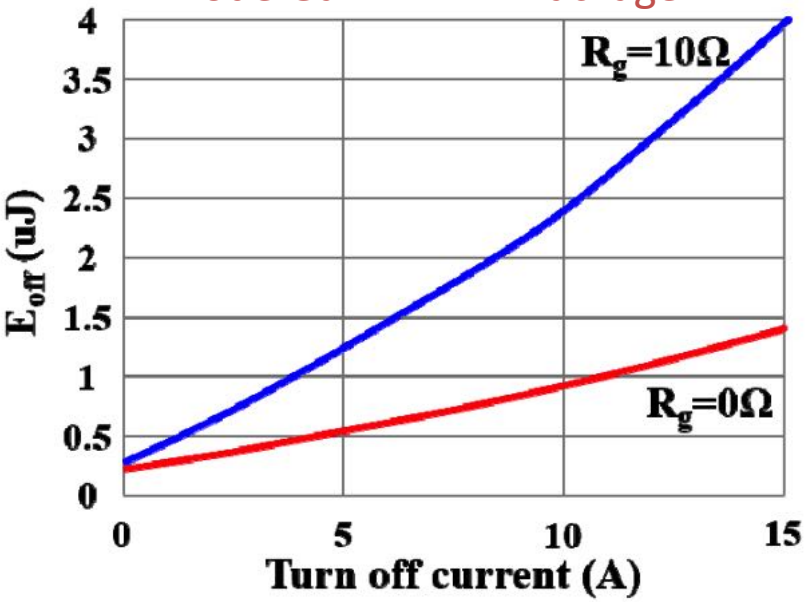
- dv/dt ↓
- di/dt ↓
- Reduces switching speed
- Increase switching loss



Gate Driving: R_g (Experimental)



E-mode GaN in DFN Package



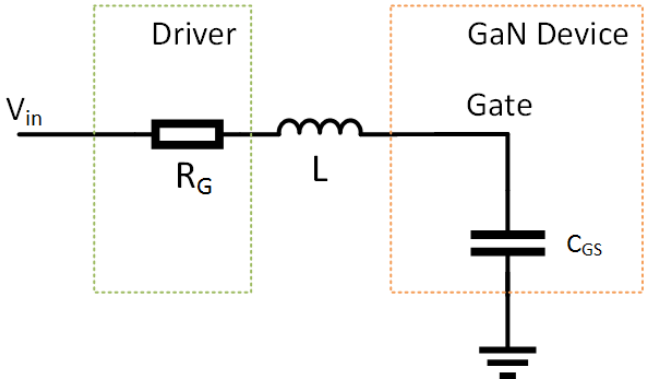
- ✓ R_g limits the gate charging and discharging current and reduces dv/dt and di/dt slew rate
- ✓ Larger R_g will increase switching loss, especially for turn-off
- ✓ A properly selected R_g can mitigate the EMI issue that stems from high switching speed

Source: X. Huang, T. Liu, B. Li, F. C. Lee, and Q. Li, "Evaluation and applications of 600V/650V enhancement-mode GaN devices," 2015 WiPDA

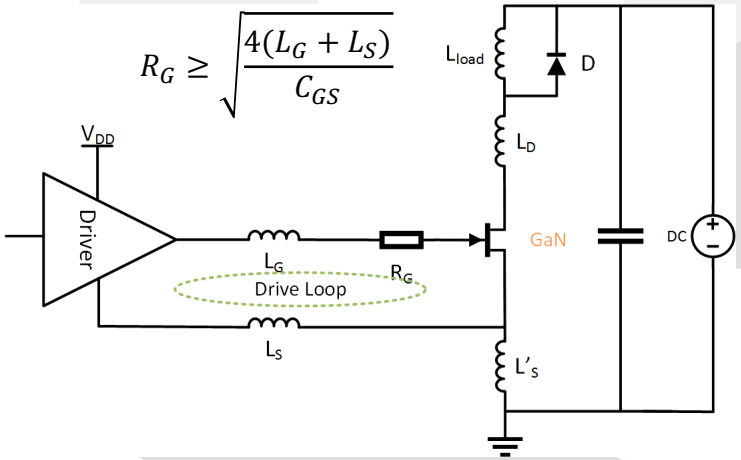
Gate Driving : R_g Design Considerations

Trade off between fast switching and ringing

- Equivalent RLC circuit for voltage driven topology:
  - Small R_G ↓ ⇒ fast switching ↑ ⇒ large ringing ↑
  - Large R_G ↑ ⇒ slow switching ↓ ⇒ small ringing ↓
- Ringing causes Conducted Electromagnetic Interference (CEMI)



$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$

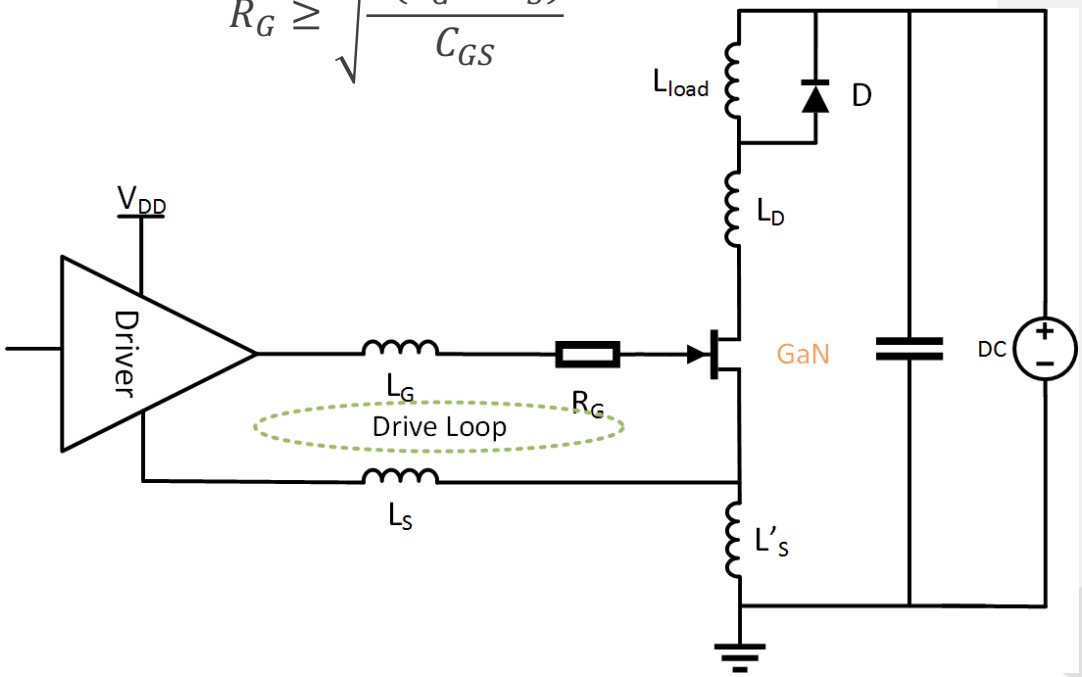


http://www.electronicdesign.com/power/take-practical-path-toward-high-performance-power-conversion

Gate Driving : R_g Design Considerations

- To avoid ringing, with certain L_G, L_S and C_{GS}, R_G can be calculated as:

$$R_G \geq \sqrt{\frac{4(L_G + L_S)}{C_{GS}}}$$



For GPI65015DFN with CGS = 119 pF

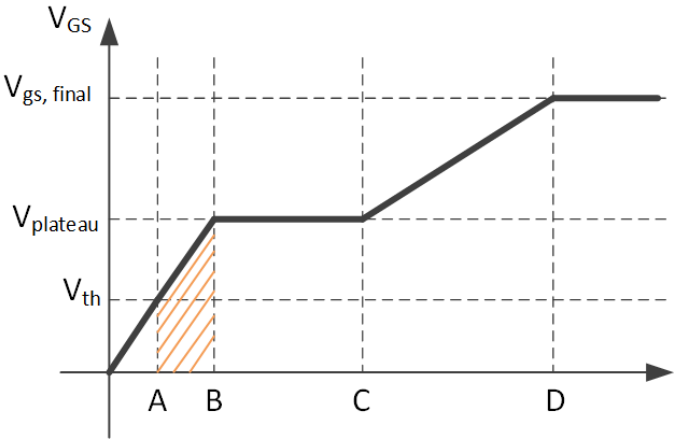
L_G+L_S (nH)	R_G (Ω)
0	0
1	5.8
2	8.2
3	10.0
4	11.6

http://www.electronicdesign.com/power/take-practical-path-toward-high-performance-power-conversion

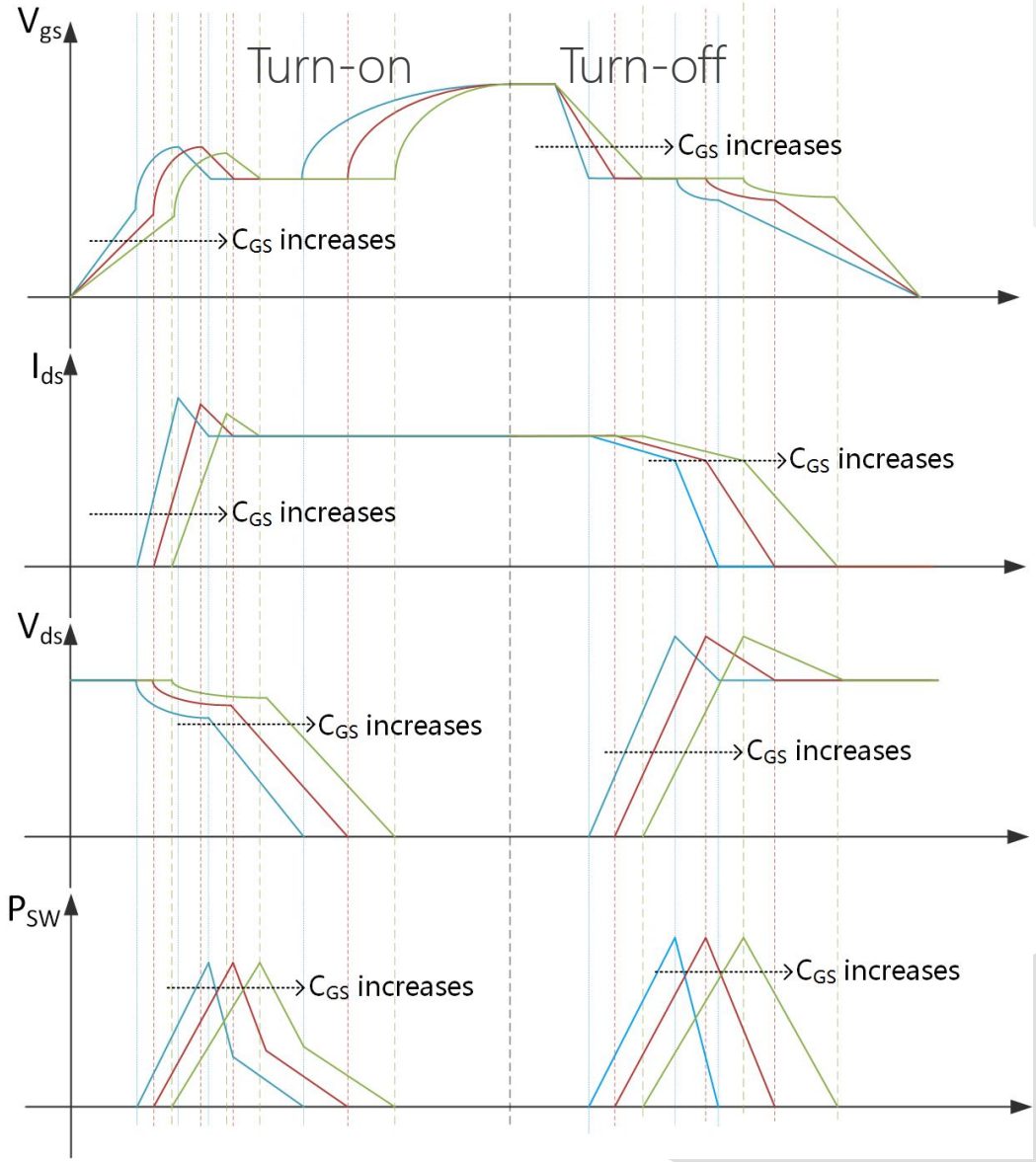
Gate Driving: C_{GS}

C_{GS} ↑:

- dv/dt -
- di/dt ↓
- C_{GS} mostly affects the current rising and falling period



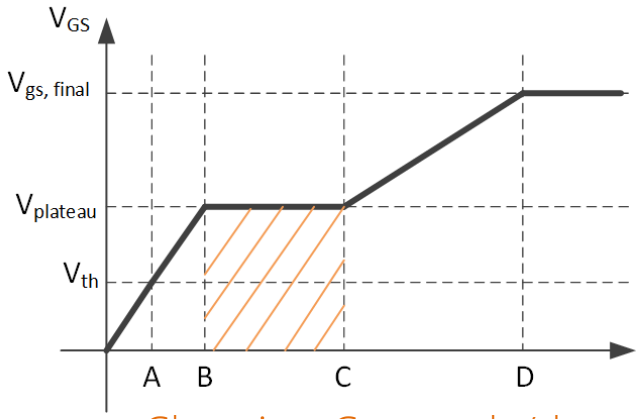
Charging C_{GS} -> di/dt



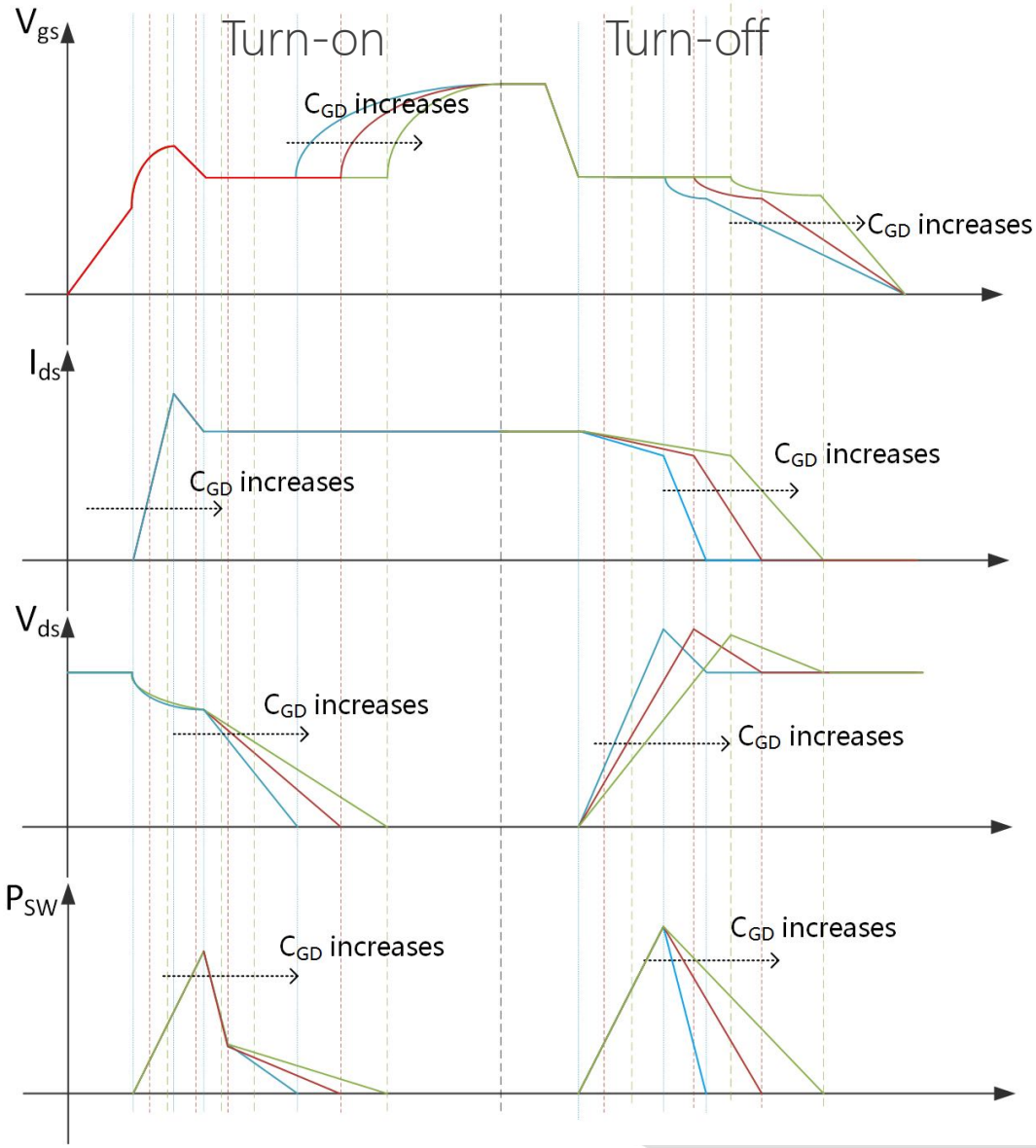
Gate Driving: C_{GD}

C_{GD} ↑:

- dv/dt ↓
- di/dt -
- C_{GD} mostly affects the drain rising and falling period during the Miller plateau

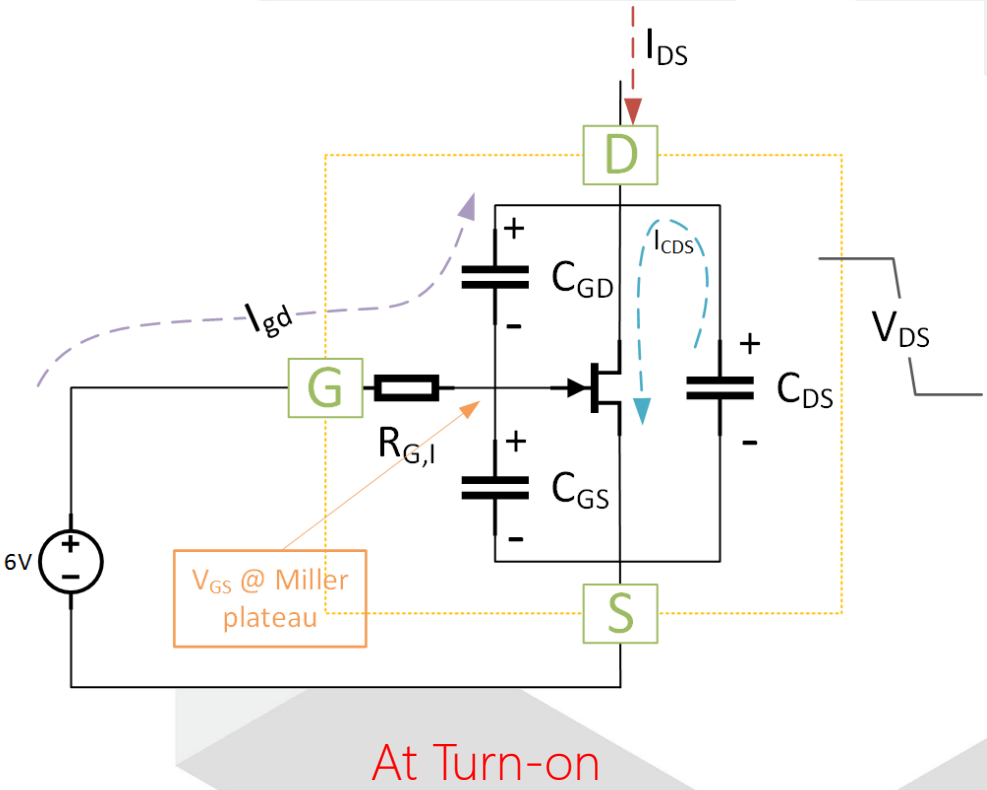


Charging C_{GD} -> dv/dt



Gate Driving: Adding External C_{DS}

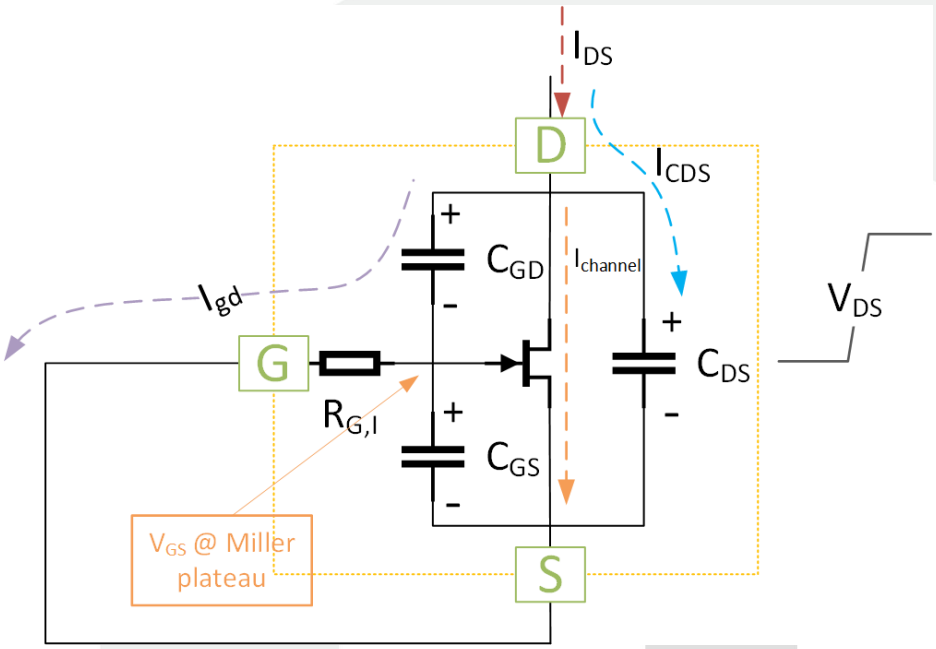
- Adding external C_{DS} capacitance does not reduce dv/dt at turn-on
- When the device turns on, at Miller plateau, drain voltage drops from V_D to 0
- dv/dt is governed by the C_{gd} and discharging current I_{gd} from the gate driver
- Paralleling external capacitance to C_{ds} doesn't impact dv/dt at turn-on, but it will add extra channel current I_{CDS} that increases switching loss for hard-switching



At Turn-on

Gate Driving : Adding External C_{DS}

- When the device turns off, at Miller plateau, drain voltage rises from 0 to V_D
- I_{DS} from the drain is diverted into three parts: I_{gd} for charging C_{GD}, I_{CDS} for charging C_{DS} and the rest goes through the channel ($I_{channel}$)
- dv/dt at turning-off is governed by C_{GD} and C_{DS}. Increasing C_{DS} will reduce dv/dt, especially if $I_{channel}$ is relatively small
- I_{CDS} will divert the current in the channel and reduces switching loss at turn-off (but increases turning-on loss at the same time for hard switching)
- If paralleling C_{DS} is required to improve EMI, the value should be large enough so that the dv/dt rate at turn-off can be modulated



At Turn-off

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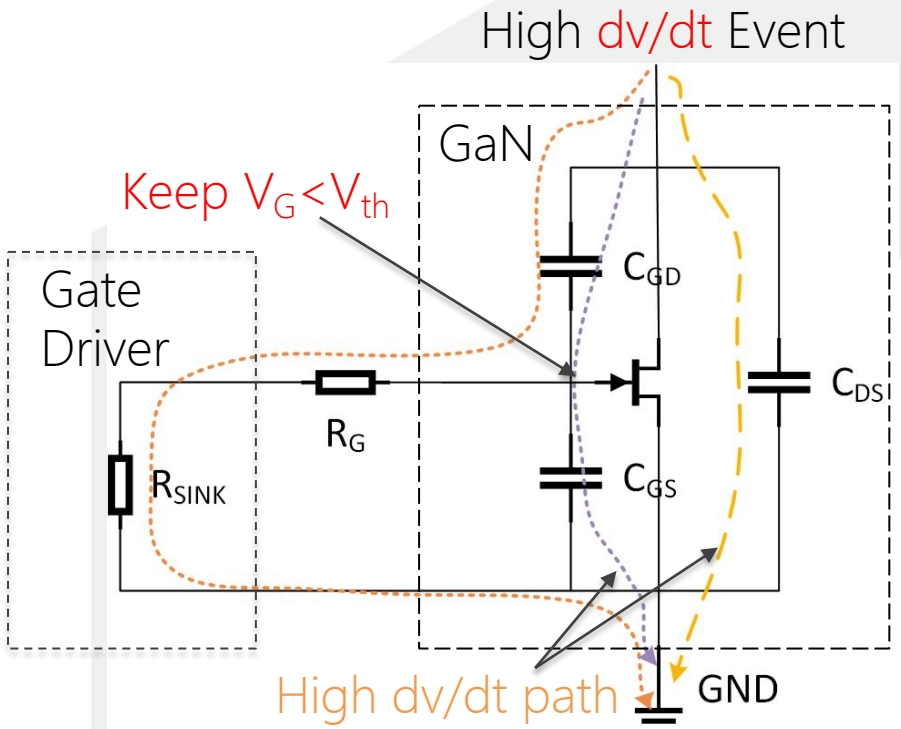
High dv/dt Effect

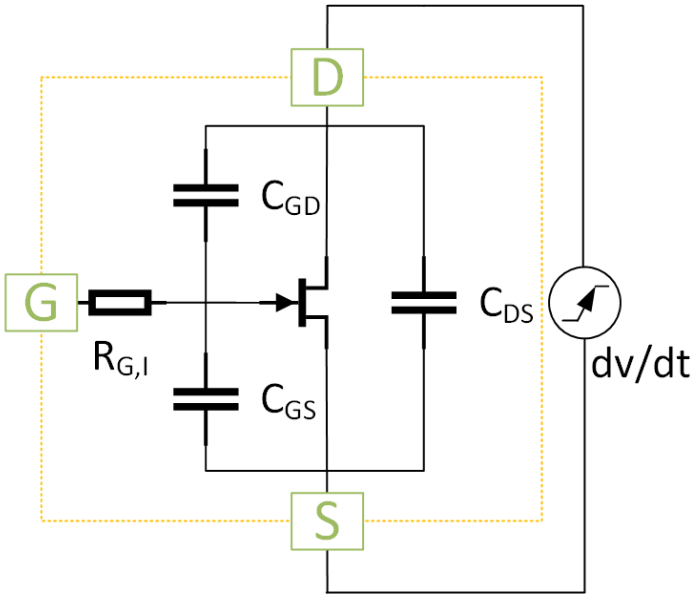
- High dv/dt charges parasitic capacitances. C_{DS} is charged during this period, as well as the series connected C_{GD} and C_{GS}
- If the V_{GS} gets higher than V_{th} due to C_{GS} charging, the device unintentionally switches on, which will lower overall efficiency. This is called Miller turn-on
- A by-pass can divert the current that flows through Miller capacitance to avoid false turn-on
- Miller ratio (Q_{GD}/Q_{GS1}) can be used to determine how fragile the devices are due to Miller false turn-on. If the ratio smaller than 1, the device is guaranteed no false turn-on, However, many commercial devices cannot keep the ratio below 1
- Miller ratio also depends on applied V_{ds}, since Q_{gd} is a function of V_{ds}. Higher V_{ds} yields larger Q_{gd} and thus more sensitive to dv/dt



Alex Lidow Johan Strydom Michael de Rooij David Reusch, GaN TRANSISTORS FOR EFFICIENT POWER CONVERSION, Wiley

GaN Device dv/dt issue: no pull-down path

With no pull-down current from external driver :



$$V_{GS} = V_{DS} \frac{C_{GD}}{C_{GS} + C_{GD}}$$

In order to maintain $V_{GS} < V_{TH}$ so that GaN device won't suffer from false turn-on, the maximum V_{DS} can be calculated as :

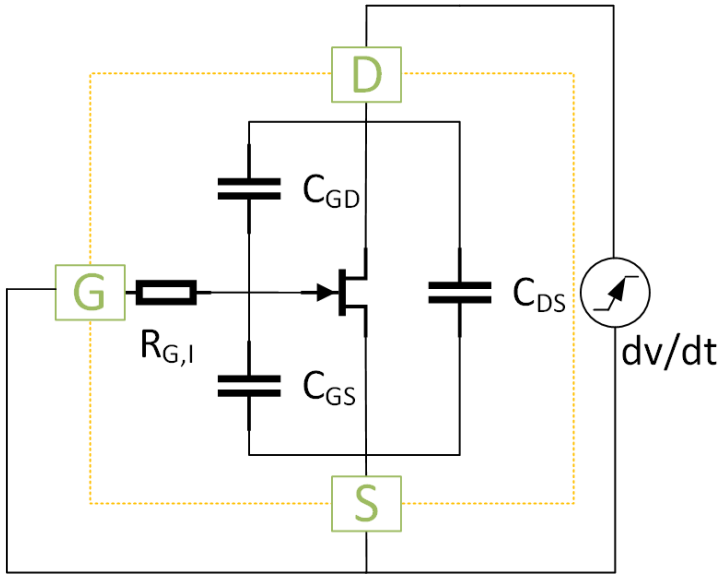
$$V_{DS,max} \leq V_{TH} \frac{C_{GS} + C_{GD}}{C_{GD}}$$

The calculated $V_{DS,max}$ value can be quite small

Texas Instruments: Estimating MOSFET Parameters from the Data Sheet

GaN device dv/dt Issue: The intrinsic dv/dt limit

If the external driver resistance is 0, which means G and S are shorted, this is to calculate the intrinsic dv/dt limit



$$C_{GD}\frac{dV_{DS}}{dt}R_{G,I} \le V_{TH}$$

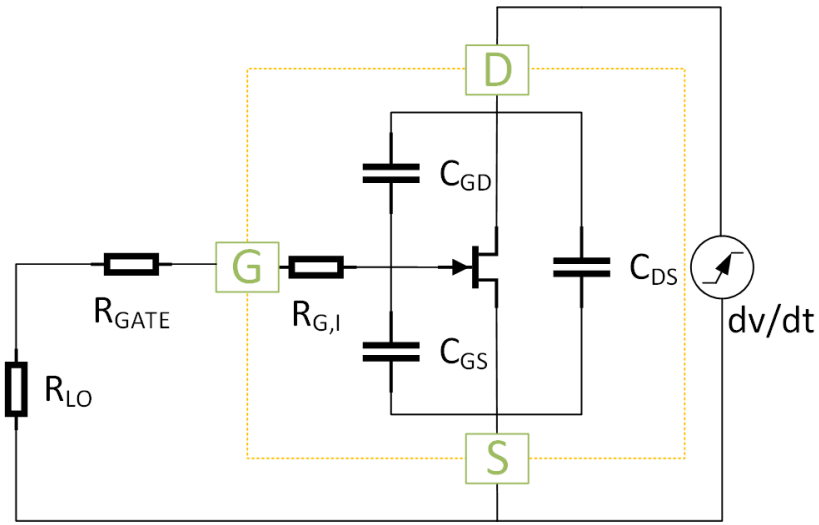
$$\Rightarrow \left.\frac{dV_{DS}}{dt}\right|_{max} \le \frac{V_{TH}}{C_{GD}\cdot R_{G,I}}$$

For example : $C_{GD} = C_{rss} = 4\ pF\ (@VDS = 400V)$; $C_{GS} = C_{iss} - C_{rss} = 123 - 4 = 119\ pF\ (@VDS = 400V)$; $R_{G,I} = 1.5\Omega$

$$\left.\frac{dV_{DS}}{dt}\right|_{max} \le \frac{V_{TH}}{C_{GD}\cdot R_{G,I}} = \frac{1.41V}{4pF\times 1.5\Omega} = 235V/ns$$

GaN device dv/dt issue: A practical design

In a practical design, with external gate resistance R_{GATE} and driver resistance R_{LO}



$$C_{GD}\frac{dV_{DS}}{dt}(R_{G,I}+R_{GATE}+R_{LO}) \le V_{TH}$$

$$\Rightarrow \left.\frac{dV_{DS}}{dt}\right|_{max} \le \frac{V_{TH}}{C_{GD}\cdot(R_{G,I}+R_{GATE}+R_{LO})}$$

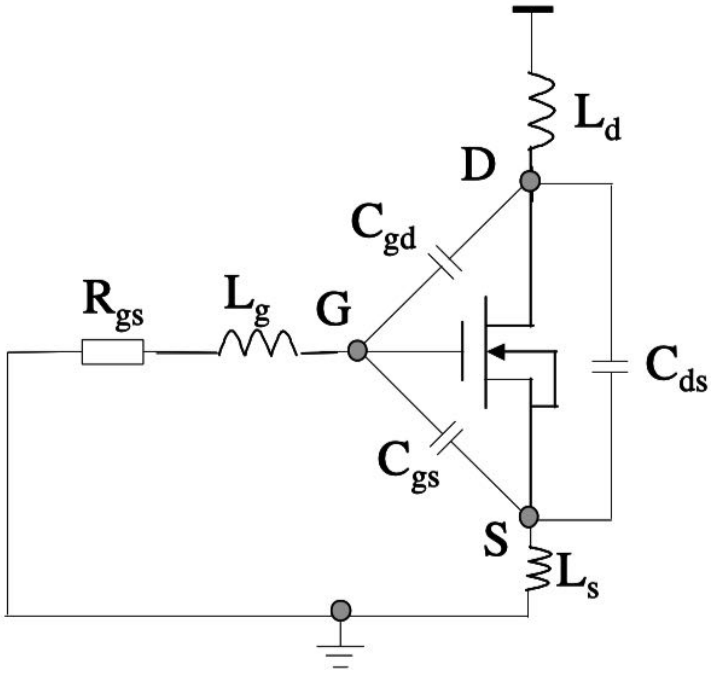
For example : $C_{GD} = C_{rss} = 4\ pF$; $C_{GS} = C_{iss} - C_{rss} = 123 - 4 = 119\ pF$; $R_{G,I} = 1.5\ \Omega$; with gate driver from TI UCC27611: $R_{LO} = 0.35\ \Omega$; and assume $R_{GATE} = 0.5\ \Omega$ and @V_{DS}=400V

$$\Rightarrow \left.\frac{dV_{DS}}{dt}\right|_{max} \le \frac{V_{TH}}{C_{GD}\cdot(R_{G,I}+R_{GATE}+R_{LO})} = \frac{1.41V}{4\ pF\cdot(1.5\Omega+0.35\ \Omega+0.5\ \Omega)} = 150V/ns$$

Low impedance turn-off drive-loop is critical for designs with GaN due to high dv/dt, especially for 650V devices

GaN device dv/dt issue: A more comprehensive approach

A more comprehensive analysis was done by a group of researchers at Virginia Tech for MOSFET before, and it can be applied to GaN as well



Besides C_{gd}, other parasitic components such as L_d, L_s, C_{gs} and C_{ds} all play a role in spurious turn-on by high drain dv/dt

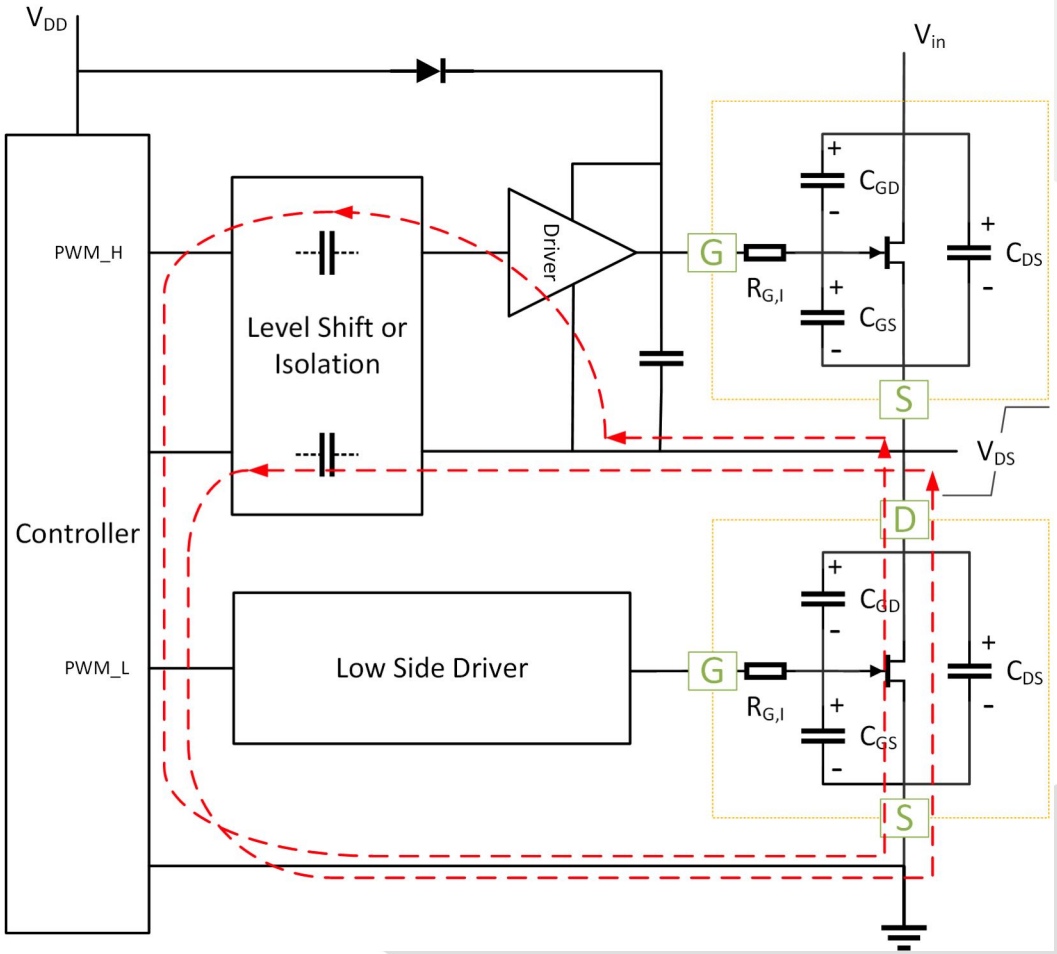
This is another reason why we should have lower parasitic inductance

$$\left.\frac{dV_{DS}}{dt}\right|_{max} \leq \frac{V_{TH}}{C_{gd}R_{gs} + C_{gd}\left(\frac{1}{C_{gs}} - \frac{R_{gs}^2}{4L_g}\right)\sqrt{(L_d + L_s)(C_{gd} + C_{ds})}}$$

Yuming Bai, Deva Pattanayak*, Alex Q. Huang, Analysis of dv/dt Induced Spurious Turn-on of MOSFET, Virginia Tech

GaN dv/dt issues: High Side

- With high positive and negative dv/dt slew rate of GaN, the common mode current can flow through the level-shifter or isolator of the high side switch
- It can cause ground bounce within the level shifter and even change logic states
- A smaller parasitic capacitance from the level-shifter or isolator is desirable, which will give a higher CMTI (common mode transient immunity)

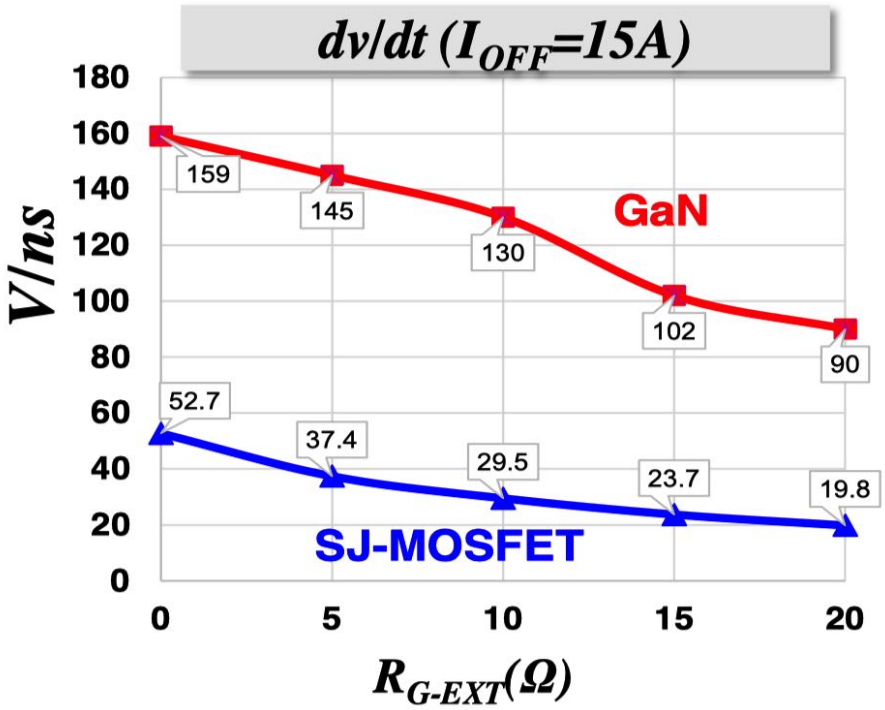


GaN vs. SJ MOS in terms of dv/dt

GaN - Cascode

State-of-Art Silicon

	Parameter	600V Si	600V GaN
Static	V_{DS}	600V	600V
	R_{DS}	0.14Ω[0]	0.15Ω[0]
Dynamic	$C_{OSS(Tr)}$	314pF[2]	71pF[2]
Reverse Operation	Q_{rr}	8200nC[3]	42nC[4]
	t_{rr}	460ns[3]	24ns[4]

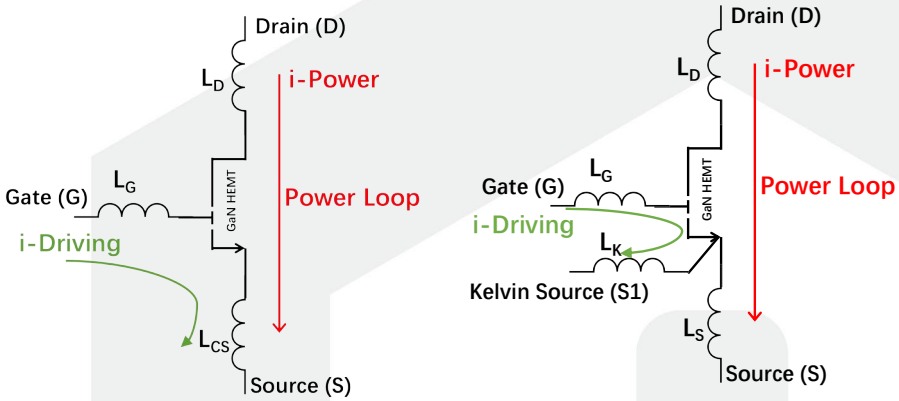


- GaN has much higher dv/dt and di/dt than SJ MOS, special designs are necessary and drivers with high CMTI (Common mode transient immunity) is necessary

Wei Zhang, A Deep Dive of Isolated Gate Driver Robustness – dv/dt (CMTI) and di/dt, TI, APEC 2018

Common Source Inductance (CSI) and di/dt issues

- The common source inductance (CSI) is shared by the power loop and the drive loop
- Voltage across the CSI will be induced by the high current slew rate di/dt during switching period
- During device turn-on, this voltage counteracts with the voltage on the gate and elongates the turn-on time
- During device turn-off, this voltage increases the gate voltage, delays the turn-off time and causes ringing and false turn-on
- This negative feedback brings longer voltage-current overlap and increases switching loss
- A Kelvin pin is generally required to separate power and driving loop

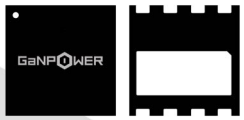


Without Kelvin Source

With Kelvin Source

Type	L_G (nH)	L_S (nH)	L_D (nH)
TO220	3.6	3.9	2.3
DFN	2.4	0.9	1.3

GaNPower TO220

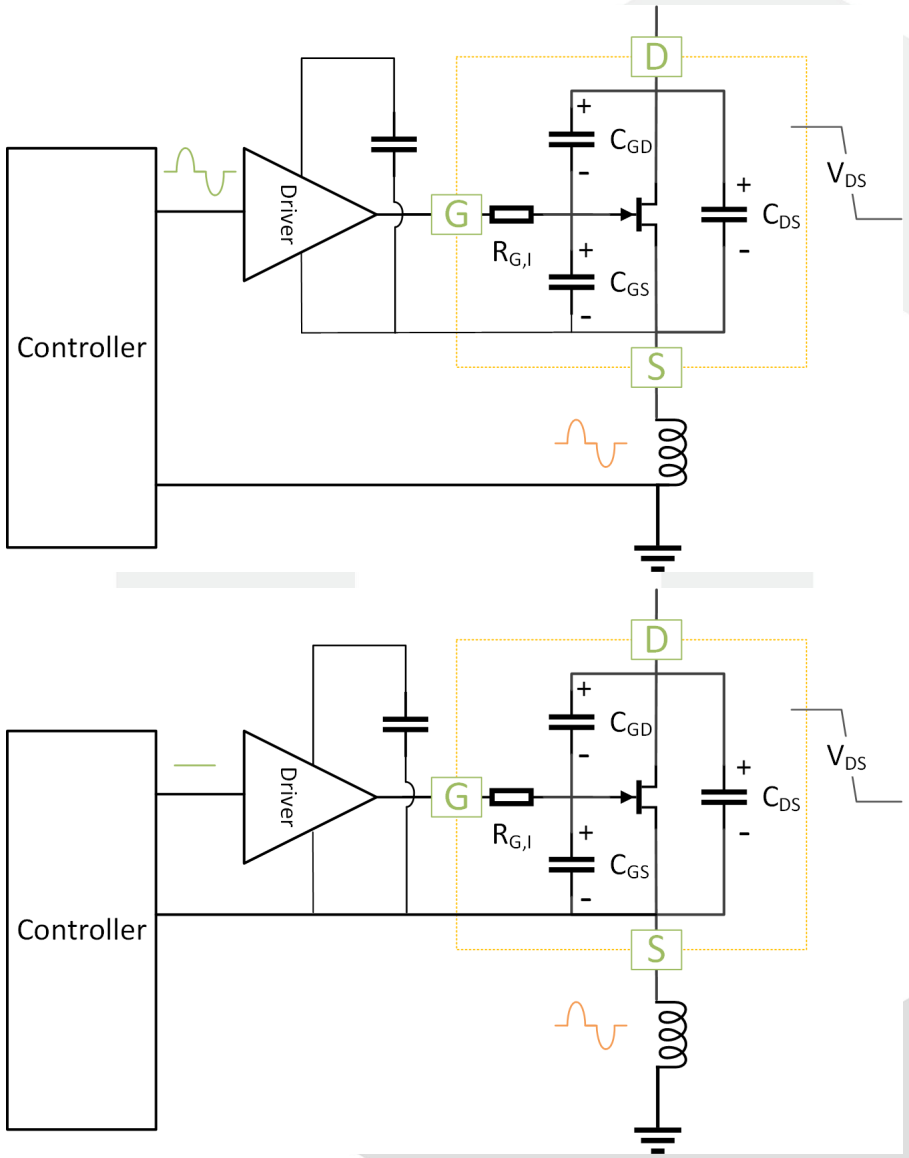


GaNPower DFN 8x8

Xiucheng Huang, Tao Liu, Bin Li, Fred C. Lee, and Qiang Li Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices , 2015 WiPDA

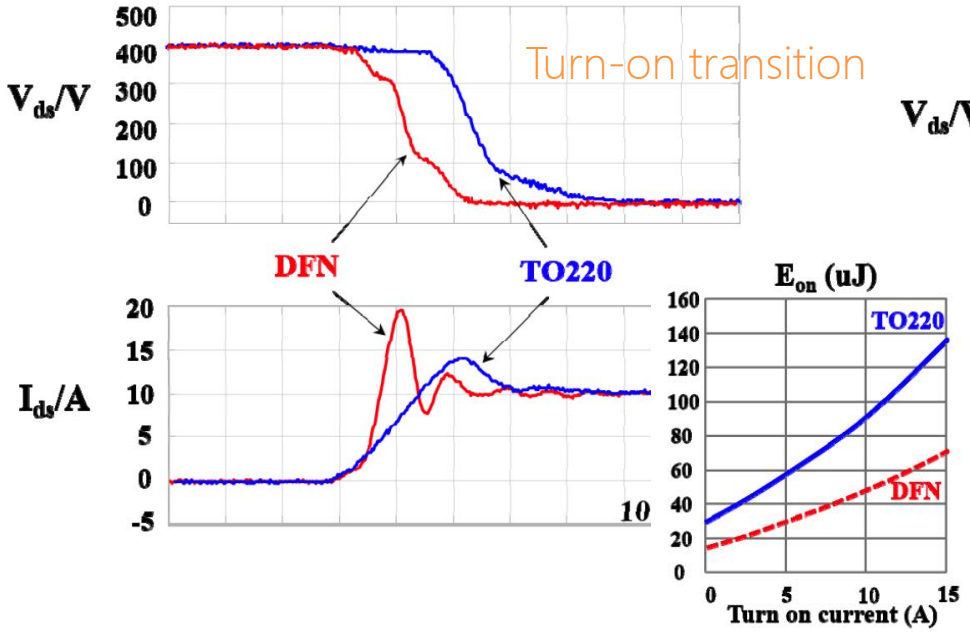
Ground Bounce

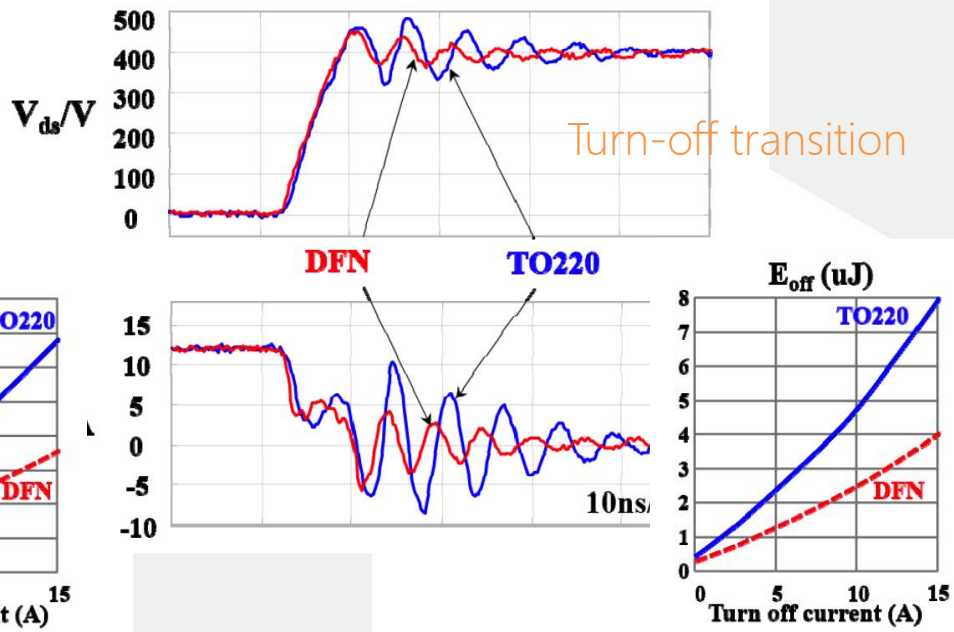
- If controller ground is tied to the power ground, the controller logic might be affected by the voltage pulses on the CSI (created by large high voltage slew rates across capacitors that generates large current pulses of short duration), which is called "ground bounce"
- Ground bounce can alter the normal device switching and lead to unwanted device behaviors
- One way to mitigate this issue is to tie the controller ground to the driver ground



Alex Lidow Johan Strydom Michael de Rooij David Reusch, GaN TRANSISTORS FOR EFFICIENT POWER CONVERSION, Wiley

DFN vs. TO220 GaN in Hard-Switching (CSI Issue)





- CSI affects di/dt, not dv/dt
- For turn-on, a lower di/dt can be observed for TO220 with CSI and no kelvin pin (due to I_g↓)
- Voltage transition is postponed due to increased current transition time
- Higher E_{on} loss for TO220

- For turn-off, there is no voltage transition delay, since voltage rises before current falls
- di/dt rate is not much different, since most of the current transition we observed are for C_{oss} charging
- However, a severe ringing occurred in TO220 that may indicate a false turn-on. E_{off} loss is higher for TO220

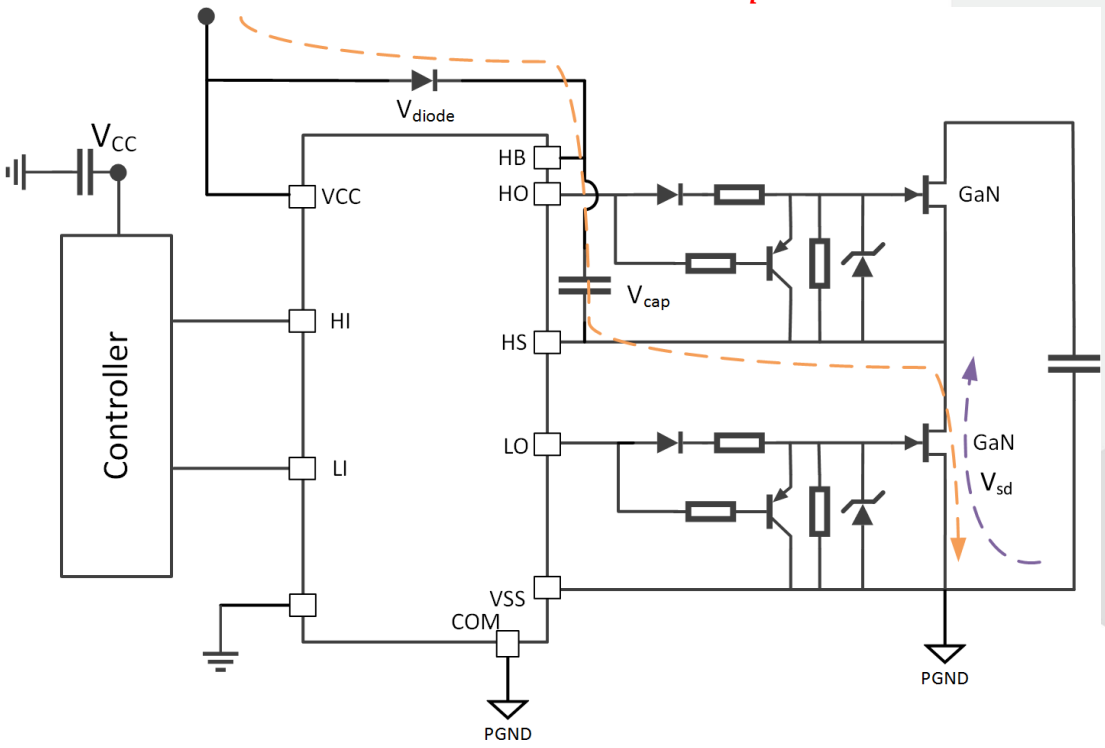
Xiucheng Huang, Tao Liu, Bin Li, Fred C. Lee, and Qiang Li; Evaluation and Applications of 600V/650V Enhancement-Mode GaN Devices, 2015 WiPDA

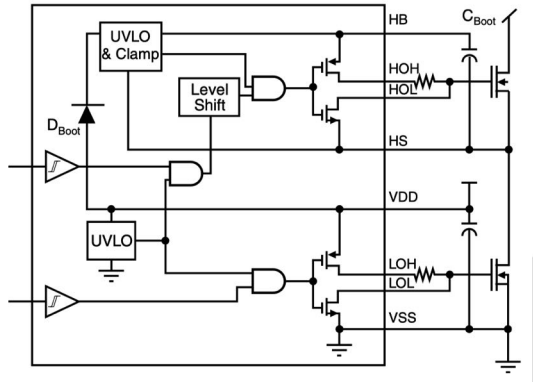
Gate Driving: Bootstrap

- If a bi-polar gate voltage (negative for turning-off) is applied, V_{sd} for GaN devices can be quite large (several Volt)
- Bootstrap capacitor can be over-charged to cause damage to upper GaN switch

Bootstrap Cap Charging

$$V_{cap} = V_{DD} - V_{diode} + V_{sd}$$





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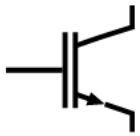
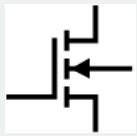
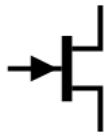
Gate Voltage Requirements

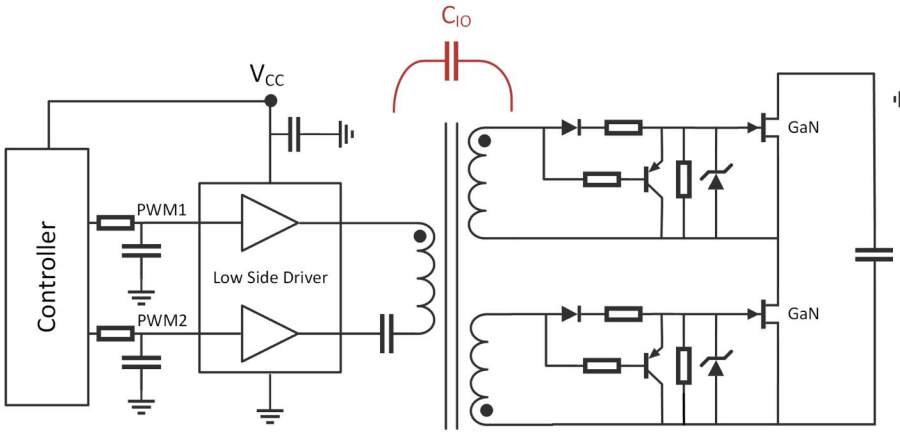
	Si-MOS	Si-IGBT	SiC-MOS	GaN
				
V_{ds} Ratings	20~650V	≥650V	≥650V	≤1200V
Optimal V_{gs}	0~+15V	-10~+15V	-5~+20V	-5~+6V
Max V_{gs}	±20V	±20V	-10~+25V	-10 ~ +7V

Commercial Discrete 650V E-Mode GaN Driver Examples

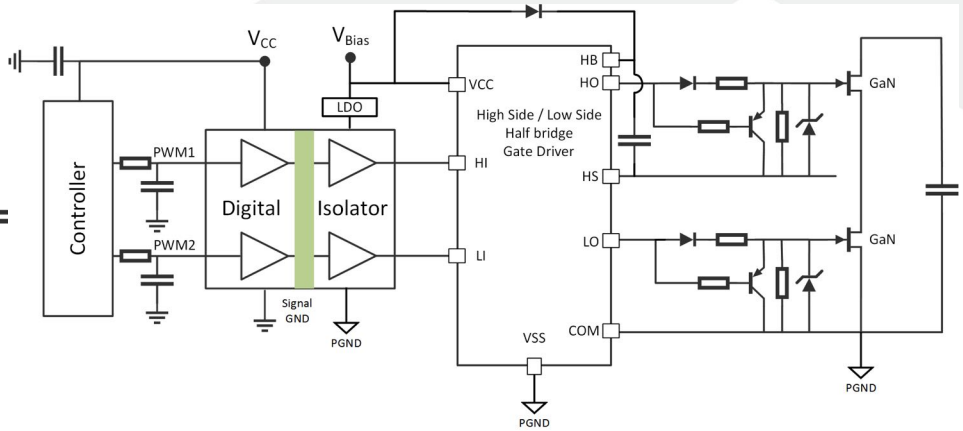
GaN Drivers	Vendor	Configuration	Sink / Source	VDD Supply Voltage	Gate Drive Voltage	Pull-up / Pull-down Resistance	Propagation Delay
LM5114	TI	Single-Sided	7.6A / 1.3A	4~12.6V	~VDD	2Ω /0.23Ω	12ns
UCC27611	TI	Single-Sided	4A /6A	4~18V	5V	1Ω /0.35Ω	14ns
UCC27517	TI	Single-Sided	4A/4A	4.5~18V	~VDD	5Ω /0.5Ω	13ns
MAX5048C	Maxim Integrated	Single-Sided	7A /3A	4~14V	~VDD	0.84Ω /0.3Ω	8ns
FAN3122	Fairchild / ON-Semi	Single-Sided	9.7A /7.1A	4.5V to 18V	~VDD	NA	20ns
Si8271	Silicon Lab	Single-Sided	4A /4A	4.2V to 30V	~VDD	2.7Ω /1Ω	60ns (max)
Si8273	Silicon Lab	Half-bridge	4A /4A	4.2V to 30V	~VDD	2.7Ω /1Ω	60ns (max)
NCP51820	ON	Half-Bridge	2A/1A	9V to 17V	5.5V	N/A	25ns

Isolated Gate Driving

In order to meet IEC 61010 isolation requirement, three types of isolated gate driving are available:

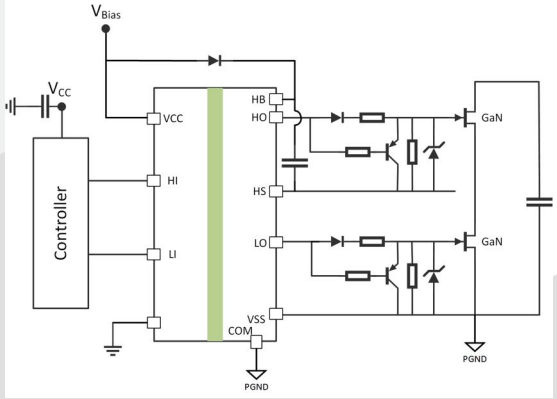


Gate Isolation with Transformer



Gate Isolation with Digital Isolator

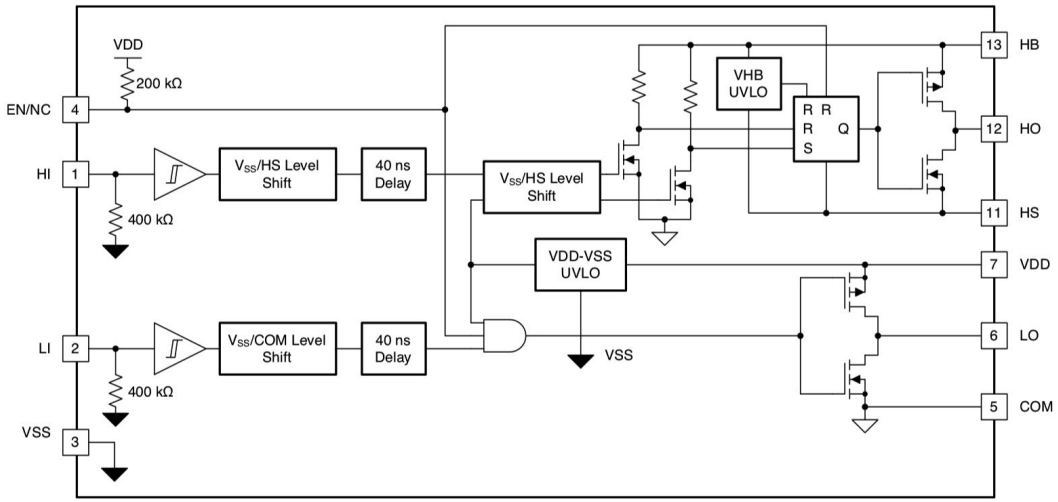
	Transformer Iso	Digital Isolator	Isolated driver
Prop. Delay	20 ns	100 ns	19 ns (Typical)
Bias Power	No	Yes	Yes
C_{IO}	≥10 pF	<1 pF	<1 pF
Parasitics	Large L_{lk}	Very Small	Very Small
Overshoot	Large	Small	Small
Size	Bulky	Small	Very Small



Isolated Gate Driver

Source: Wei Zhang, Mastering the art and fundamentals of high voltage gate driver; TI High Volt Interactive

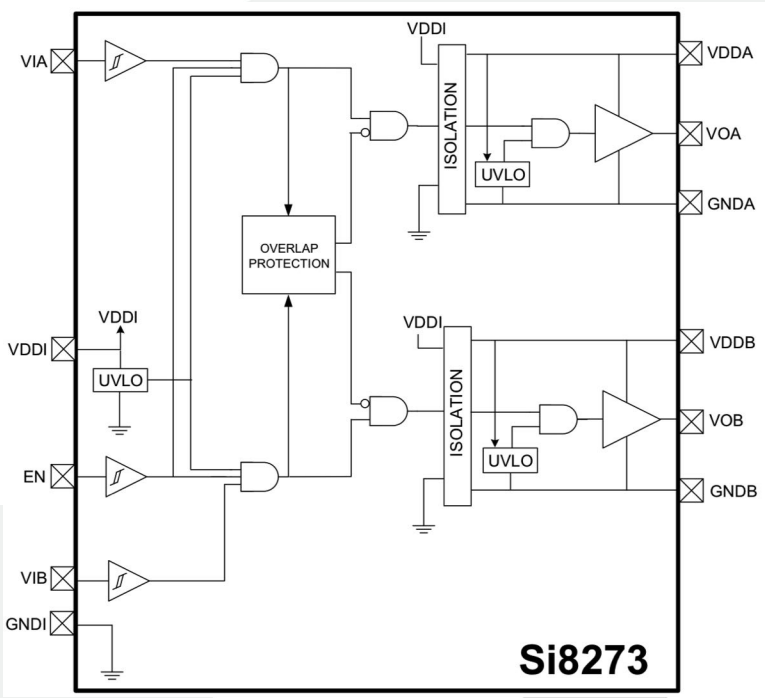
Half Bridge Gate Driver : Isolated and Non-Isolated



A typical non-isolated gate driver from TI

Isolated gate driver such as Si8273 provides:

- ✓ 200 kV/μs CMTI
- ✓ 2.5 kV RMS withstand voltage
- ✓ Input supply: 2.5–5.5 V
- ✓ Driver supply: 4.2–30 V (6V for E-mode GaN)
- ✓ Prop. Delay: 60 ns (max)



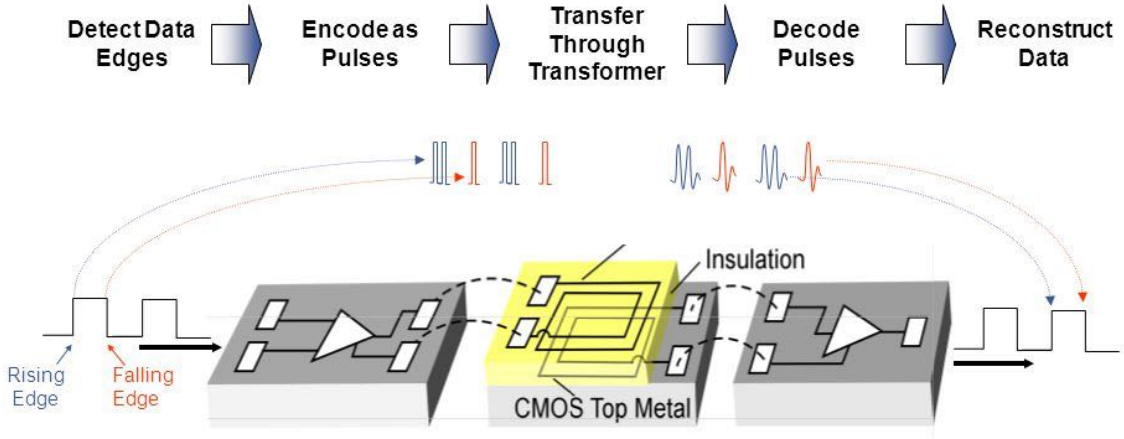
A typical isolated gate driver from Silicon Lab for GaN

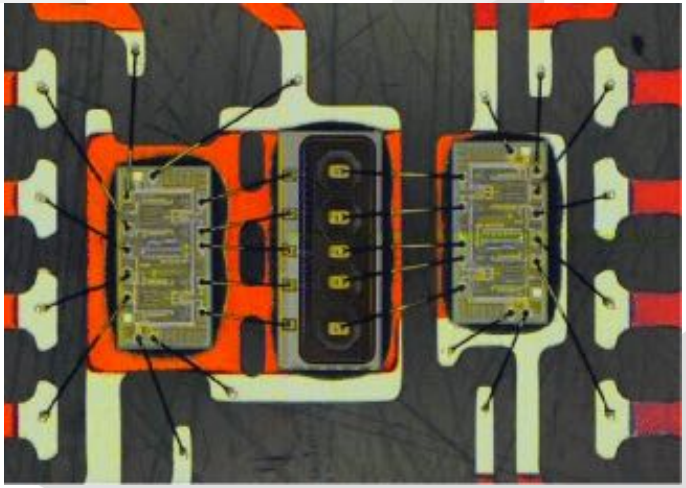
UCC27714High-Speed, 600-VHigh-SideLow-SideGateDriver with 4-A Peak Output
https://www.silabs.com/documents/public/data-sheets/Si827x.pdf

Digital Isolation Technology: Magnetic Isolator

Magnetic isolator is based on chip-scale transformers, compared to optocoupler, magnetic couplers use low-stress, thick-film polyimide insulation to achieve thousands of volts of isolation that can be monolithically integrated with standard silicon ICs and can be fabricated in single-channel, multi-channel, and bidirectional configurations

- ✓ 4x improvement in data rate and timing specifications
- ✓ Integrates multiple isolation channels with other functions to reduce size and cost
- ✓ Operates at power levels up to 90% lower than optocouplers
- ✓ Minimizes external components needed to connect to other digital devices
- ✓ Increases reliability by eliminating LEDs used in optocouplers

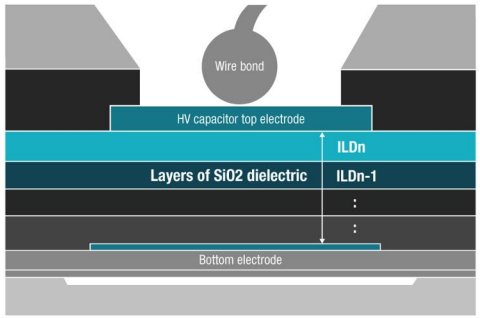


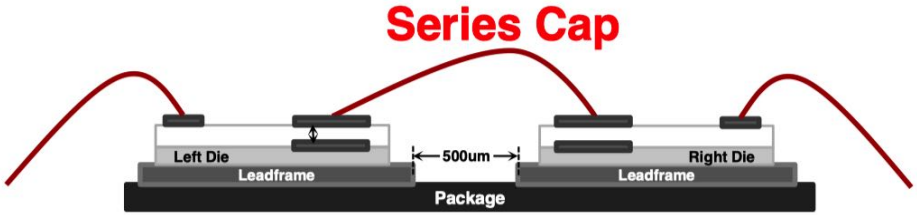


Ref: Analog Devices: Standard Digital Isolators

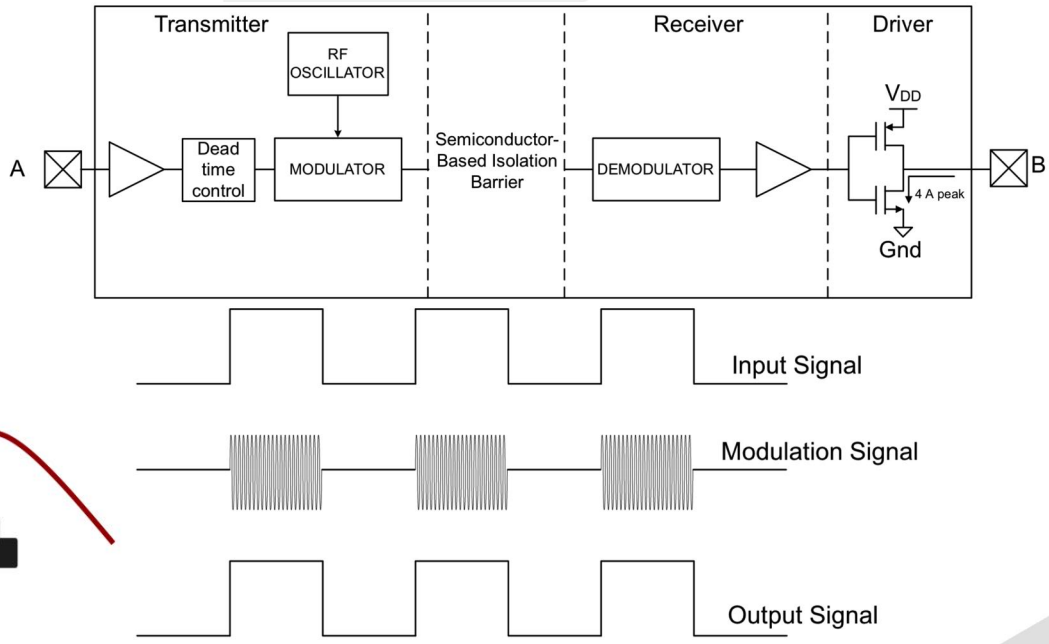
Digital Isolation Technology: Capacitive Isolator

Capacitive isolation is made by adding capacitive isolation barrier on top of each die to connect in series, digital circuits are used for encoding and decoding various signals through the isolation barrier. A capacitive isolator's inability to pass DC signals makes it inherently the right choice for isolation





TI's capacitive isolation barrier is made from layers of high-dielectric SiO_2

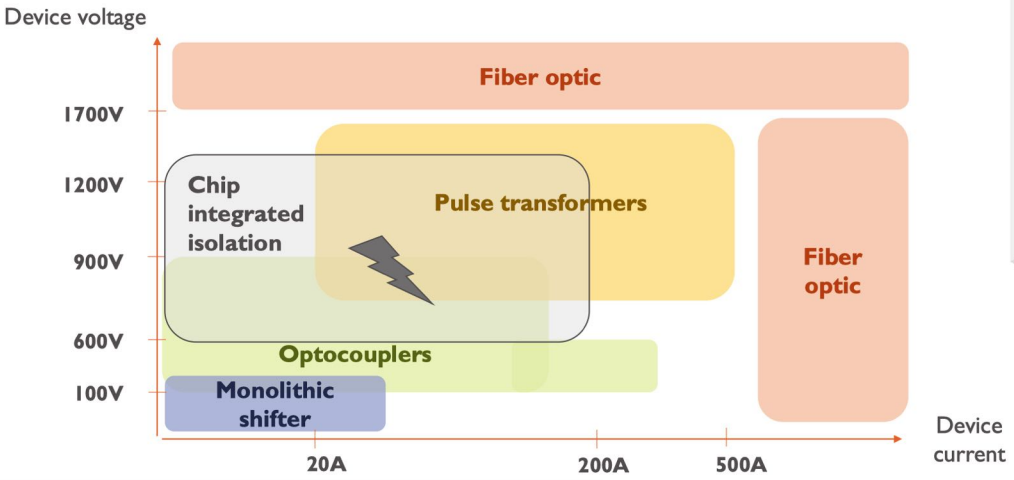


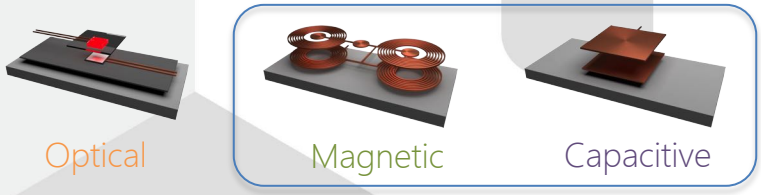
Silicon Lab's capacitive isolation solution

1, Capacitive Isolation: The Future AC/DC Power Conversion, Monolithic Power Systems
2, https://www.silabs.com/documents/public/data-sheets/Si827x.pdf
3, TI: Digital Isolators

Isolation Technology: Comparison

	Isolation	dv/dt immunity	Propagation delay	Integration level	Independent power supply needed at the secondary	Reliability (over time & harsh environment)	Cost
Optocouplers	Few kV	>50kV/µs	>400ns	Medium	Yes	Aging issues	$
Fiber optic	Several 10's kV	>100kV's/µs	Negligible	Medium	Yes	Good reliability	$$$$
Monolithic level shifter	None	50kV/µs	-	Integrated on the IC	No	-	$
Pulse transformer	Several kV	>50kV/µs	<100 ns	Bulky	No	Reliable	$
Digital isolation	Several kV	>100kV/µs	~20 ns	Integrated on-chip or driver IC package	Yes	Very reliable	$$



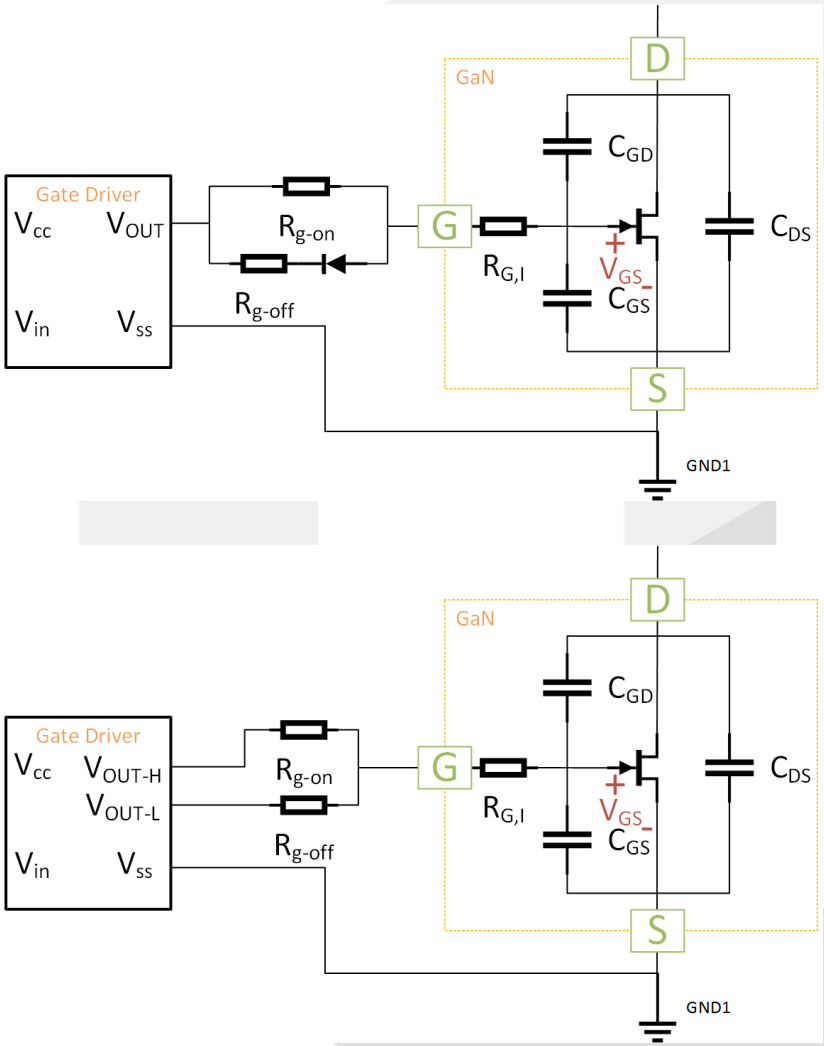


Chip Integrated Isolation

Source:
Gate Drivers market evolution: coreless isolation and WBG specific solutions, Yole Development, APEC 2018

Choosing GaN Gate Driver and R_g

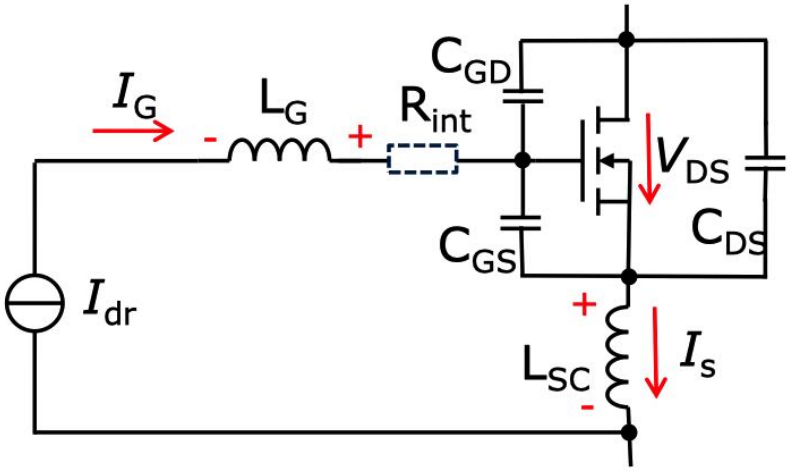
- If possible, gate drivers with individual turn-on and turn-off pins are recommended
- Use separate drive loops for turn-on and turn-off. Turn-off loop low impedance is recommended to avoid false turn-on and oscillations
- Proper selection of $R_{g\text{-}on}$ vs. $R_{g\text{-}off}$ is critical. Normally the ratio of $R_{g\text{-}on}$ to $R_{g\text{-}off}$ can be chosen between 5 to 10

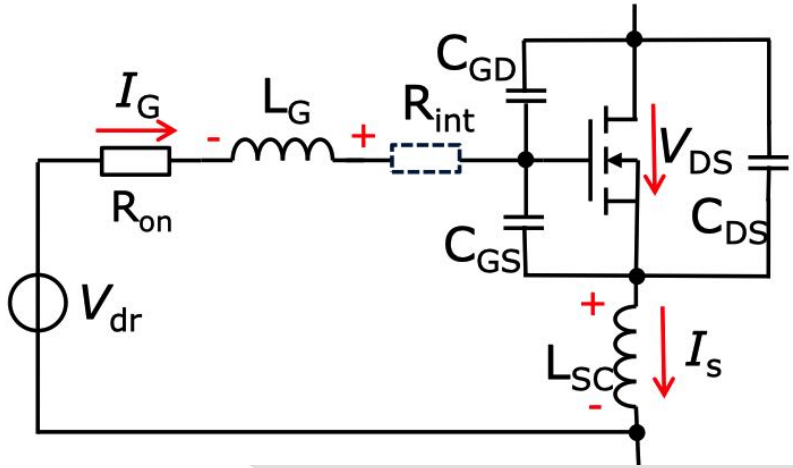


*Source: GN001 Application Guide: Design with GaN Enhancement mode HEMT, GaN Systems

Current-source and Voltage-source Gate Drivers

Current-source gate driver	Voltage-source gate driver
➢ Current sources have a high resistive output by default	➢ Voltage sources shall be as low resistive as possible
➢ Any additional voltage drop in the gate drive loop has no influence on the gate current I_g inside limits	➢ Any additional voltage drop in the gate drive loop has immediate influence on the gate current I_g
➢ Supposed to damp oscillations	➢ Prone to oscillations





Ref: Turn-on performance comparison of current-source vs. voltage-source gate drivers, Infineon, APEC 2018

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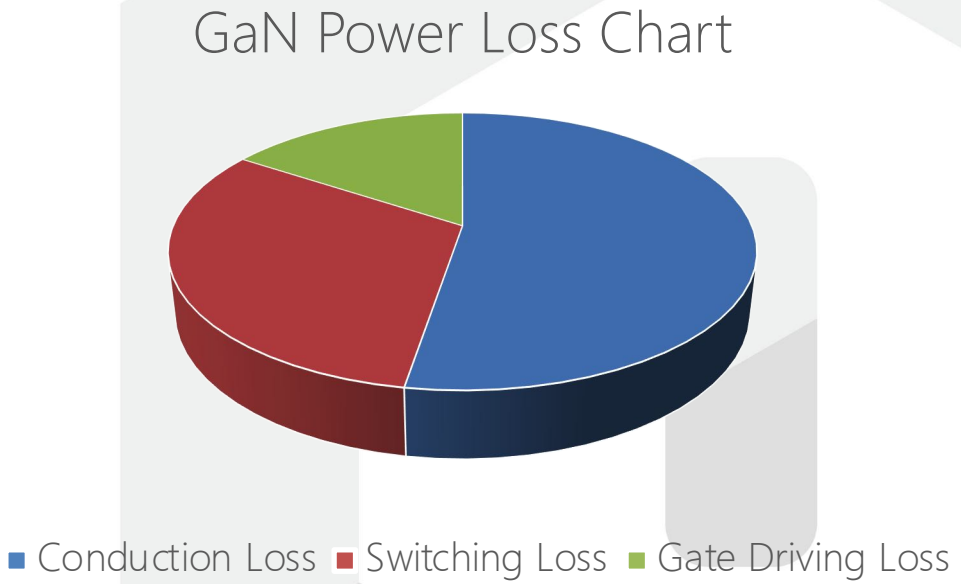
GaN Device Power Loss Analysis

- **Conduction Loss:**
  $P_{Cond}=I_D^2 \cdot R_{dson} \cdot D$ (D: Duty Cycle)

- **Switching Loss:**
  $P_{Switching}=1/2 \cdot I_D \cdot V_D \cdot (t_{on}+t_{off}) \cdot f_{sw}$

- **Gate Driving Loss:**
  $P_{Driving}=V_g \cdot Q_g \cdot f_{sw}$

- **Power Loss from C_{oss}**
  $P_{COSS}=E_{OSS} \cdot f_{sw}$

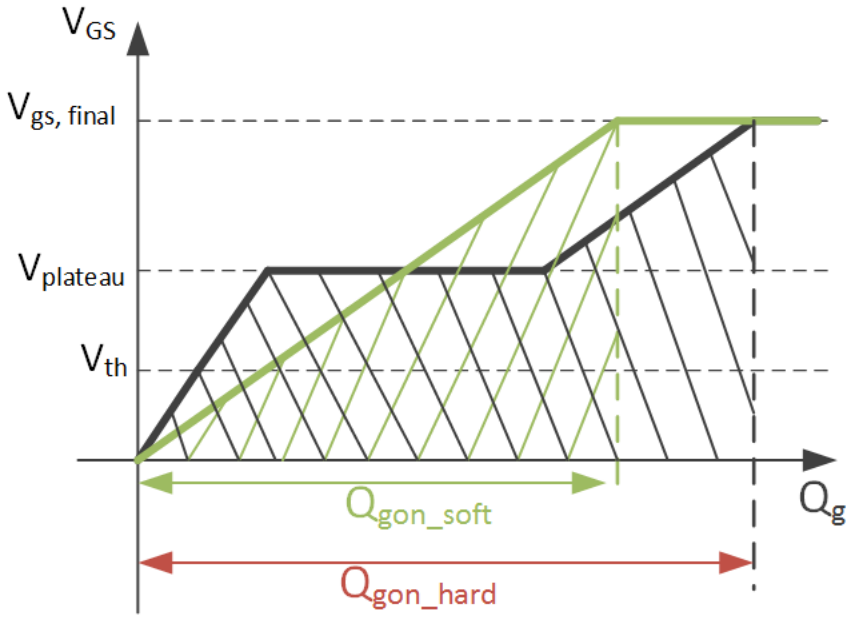


GaN Gate Driving Loss

With same gate driver, soft-switching such as ZVS has a lower turn-on gate driving loss than hard-switching:

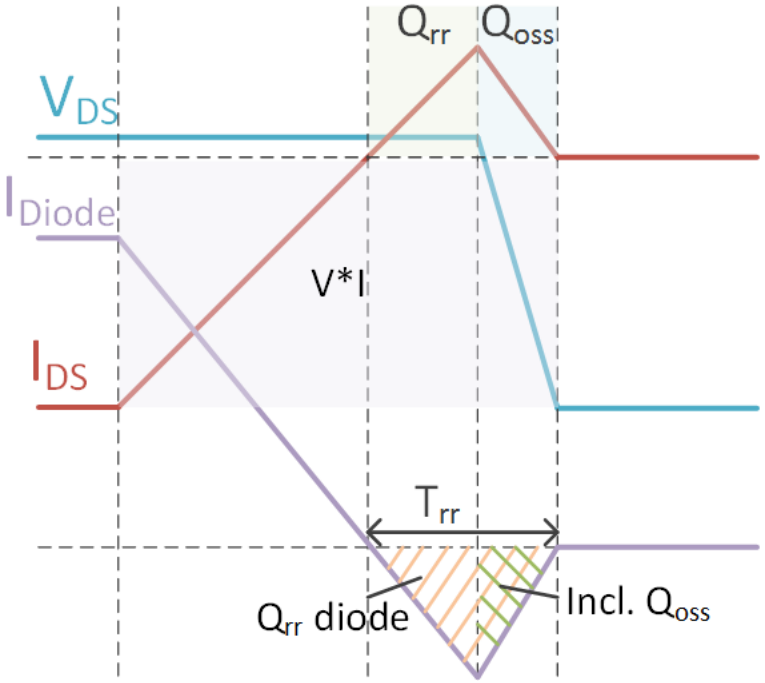
$$P_{gate\_dr\_on} = E_{on\_soft} \cdot f_{sw} = V_{gs} \cdot Q_{gon\_soft} \cdot f_{sw}$$

$$P_{gate\_dr\_on} = E_{on\_hard} \cdot f_{sw} = V_{gs} \cdot Q_{gon\_hard} \cdot f_{sw}$$

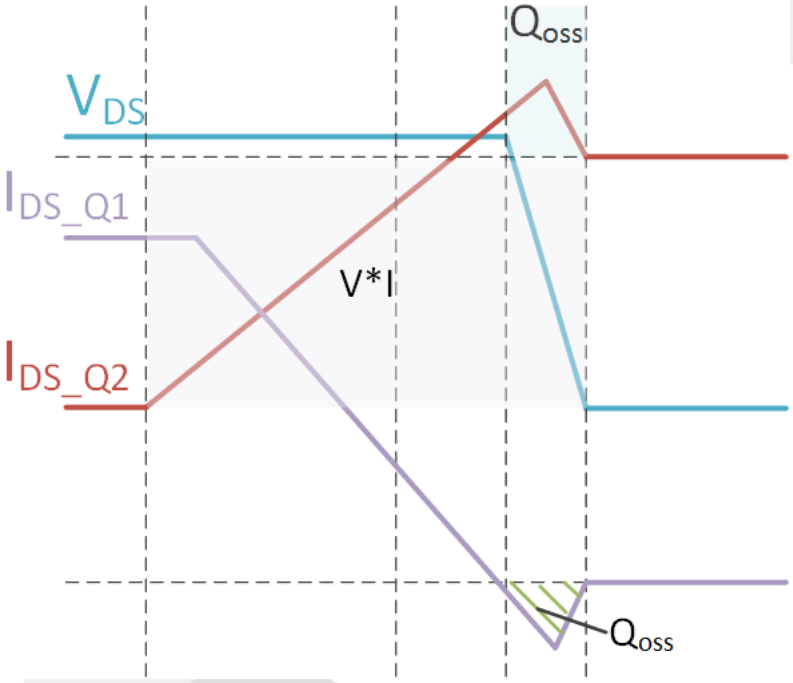


Wei Zhang, Mastering the art and fundamentals of high voltage gate driver; TI High Volt Interactive

GaN vs. SJ MOS: Q_{rr} and Q_{oss} Loss



SJ MOSFET with Q_{rr} from body-diode and Q_{oss}



GaN HEMT with Q_{oss} from other GaN

Peter Di Maso, Lucas Lu, GaN E-HEMTs Enable Innovation in Power Switching Applications, GaN Systems, APEC 2017

GaN Device Power Loss Analysis: Hard-Switching

- With same R_{dson} and same frequency, GaN power loss vs. Si:

$$P_{hard\_sw} = P_{cond} + P_{sw} + P_{coss} + P_{gate} + P_{sd} + P_{rr}$$

	SJ MOS	GaN	Remark
P_{cond}	same	same	Same R_{dson}
P_{sw}	higher	lower	Due to GaN has smaller Q_{GS2} and Q_{GD}
P_{coss}	higher	lower	GaN has a lower C_{oss}
P_{gate}	higher	lower	GaN has lower gate drive voltage
P_{sd}	lower	higher	GaN has a higher V_{sd}
P_{rr}	higher	none	GaN has no Q_{rr}
P_{hard_sw}	higher	lower	GaN has a lower total hard switching power loss

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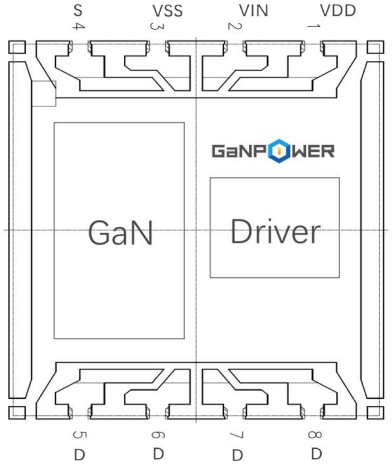
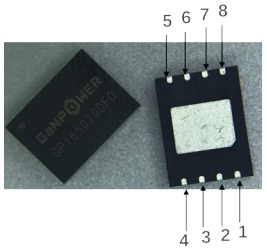
Si Driver + GaN Co-package





PARAMETER		TEST CONDITION		MIN TYP MAX	UNIT
V_{DD} (V_{DD} operating voltage)		(T_J) range of –40°C to 125°C		5	V
UVLO	V_{DD} under voltage lockout	V_{DD} Rising	T_j=25°C	3.8	V
	V_{DD} undervoltage lockout hysteresis			0.2	
I_{DD} (V_{DD} quiescent current)		I_N=I_{NB}=0	T_j=25°C	0.01	mA
N-CHANNEL OUTPUT					
R_{on-N} (Driver output resistance-pulling down)		V_{DD} = 5V, I_{N-OUT} = –100mA		0.25	Ω
I_{PK-N} (peak sink current)		C_L = 10,000 pF		5	A
P-CHANNEL OUTPUT					
R_{on-P} (Driver output resistance-pulling up)		V_{DD} = 5 V, I_{N-OUT} = 50 mA		2.1	Ω
I_{PK-P} (peak source current)		C_L = 10,000 pF		1.3	A

GPI65030CO: Si driver basic parameters

GPI65030CO: double-pulse test, rising edge of second pulse (turn-on @ second pulse). Yellow: Drain to Source Voltage; Blue: Drain to Source Current

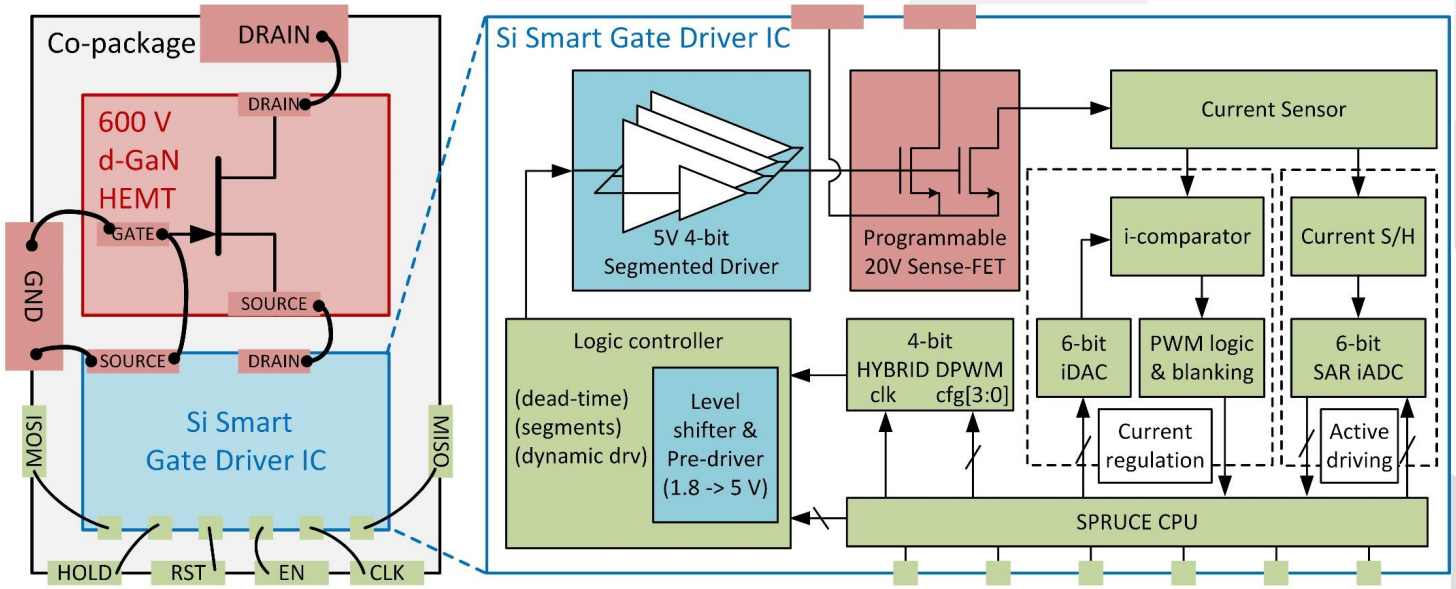
PARAMETER	TEST CONDITION (VDD=5V)		MIN TYP MAX	UNIT
t_R Rise time	C_L=1nf		5	ns
t_F Fall time	C_L=1nf		3	ns
t_{D-ON} turn-on propagation delay	C_L=1nf	T_j=25°C	17	ns
		(T_J) range of –40°C to 125°C	12.9 20	
t_{D-OFF} turn-off propagation delay	C_L=1nf	T_j=25°C	15.7	ns
		(T_J) range of –40°C to 125°C	13.5 18	

GPI65030CO: Si driver dynamic parameters

Si Driver + GaN Co-package: D-Mode GaN

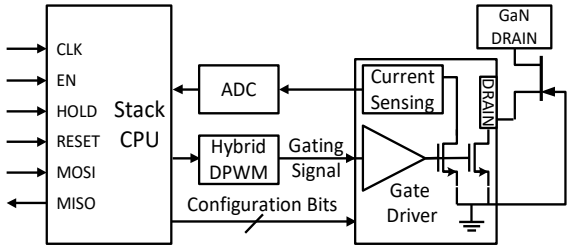
A smart gate driver IC for cascode D-GaN (By University of Toronto)

- ✓ Desired functions include
  - ✓ Tunable output resistance
  - ✓ Precise timing control
  - ✓ Current sensing for regulation and protections purposes
- ✓ Dynamic driving techniques
  - ✓ Change gate driving strength during switching
- ✓ Fully integrated controller circuits
  - ✓ Flexible digital control
  - ✓ Active driving ability under different load conditions

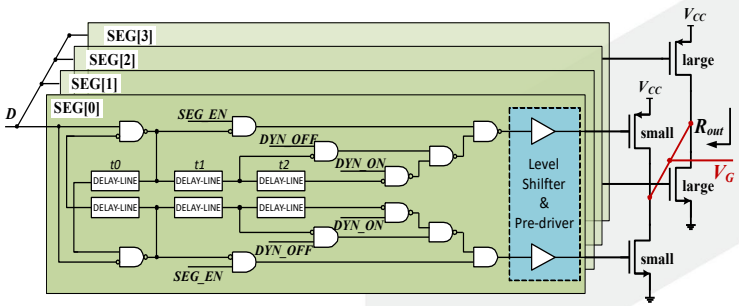


Jingshu Yu, Weijia Zhang, Andrew Shorten, Rophina Li and Wai Tung Ng, A Smart Gate Driver IC for GaN Power Transistors; ISPSD 2018

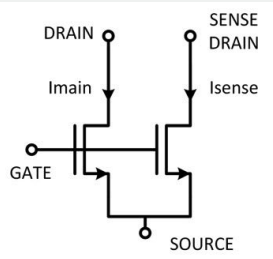
Si Driver + GaN Co-package: D-Mode GaN



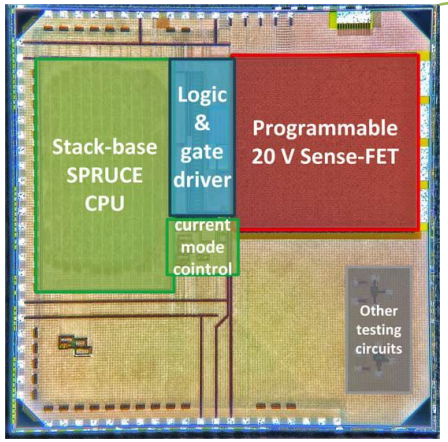
On-chip Digital Controller



Segmented Gate Driver

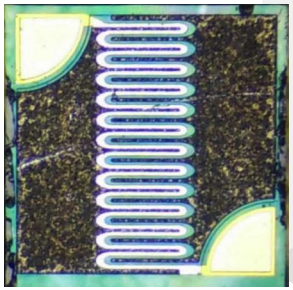


Programmable sense-FET



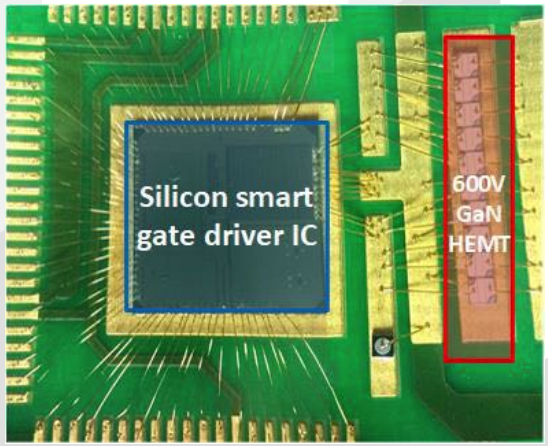
Smart Gate Driver IC

+



10X D-Mode GaN by GaNPower

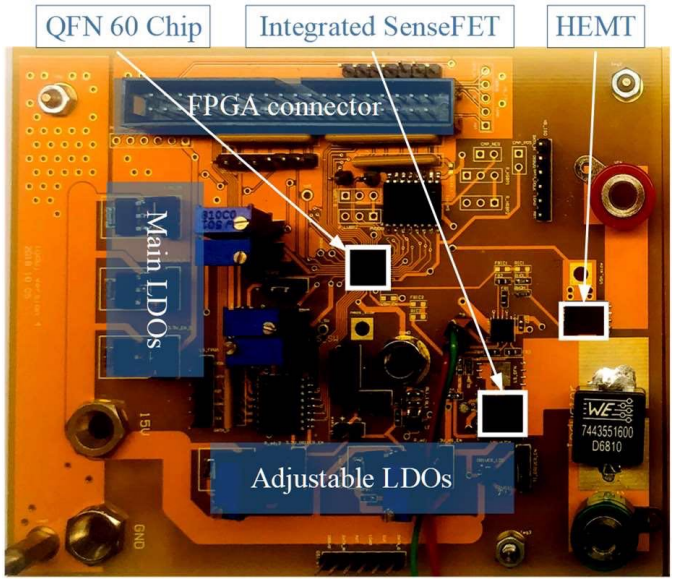
=



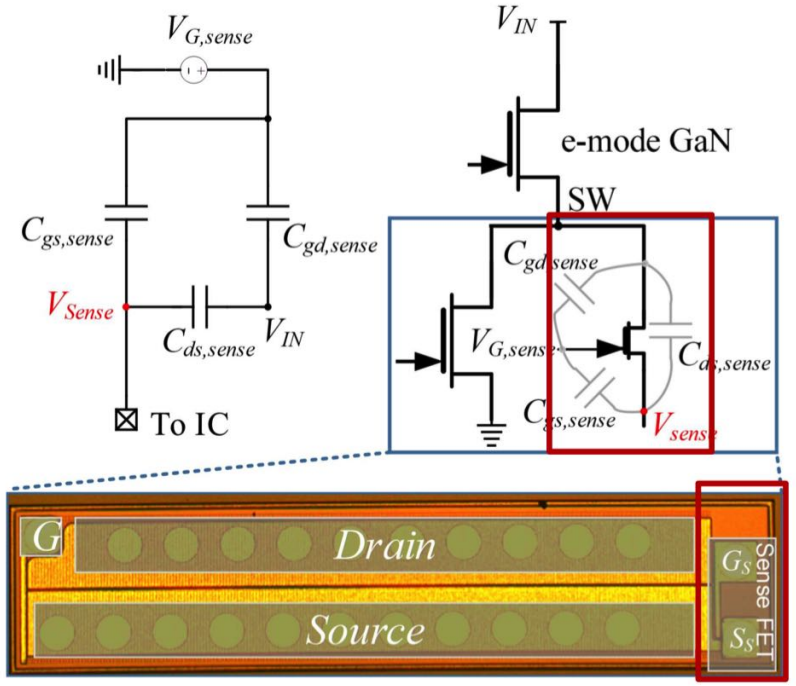
Jingshu Yu, Weijia Zhang, Andrew Shorten, Rophina Li and Wai Tung Ng, A Smart Gate Driver IC for GaN Power Transistors; ISPSD 2018

Si Driver + GaN Co-package: E-GaN and SenseFET

A novel SenseFET by GaNPower helps researchers from University of Toronto won the prestigious 2019 IEEE ISPSD Charitat Young Researcher Award



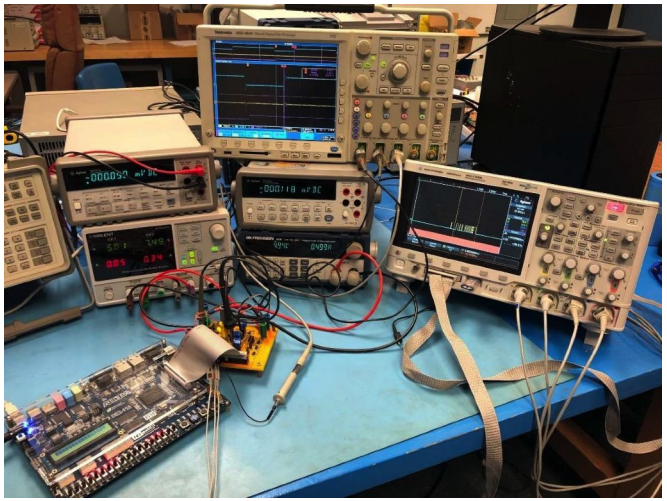
Integrated GaN SenseFET



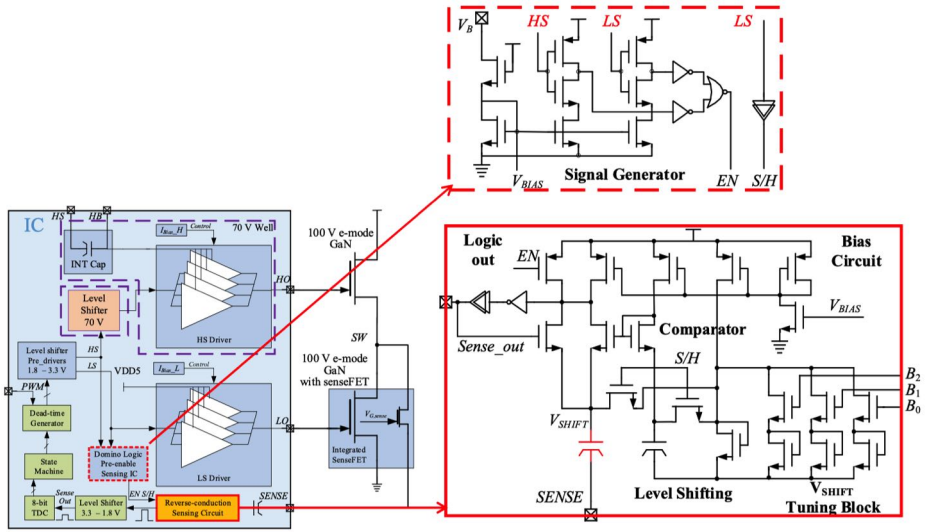
GaNPower SenseFET GaN, in collaboration with University of Toronto

Source: W.J. Zhang, Y.H. Leng, J.S. Yu, Y.S. Lu, C.Y. Cheng and W.T. Ng, A Gate Driver IC for Enhancement Mode GaN Power Transistors with Precise Dead-time Correction, ISPSD 2019

Si Driver + GaN Co-package: E-GaN and SenseFET



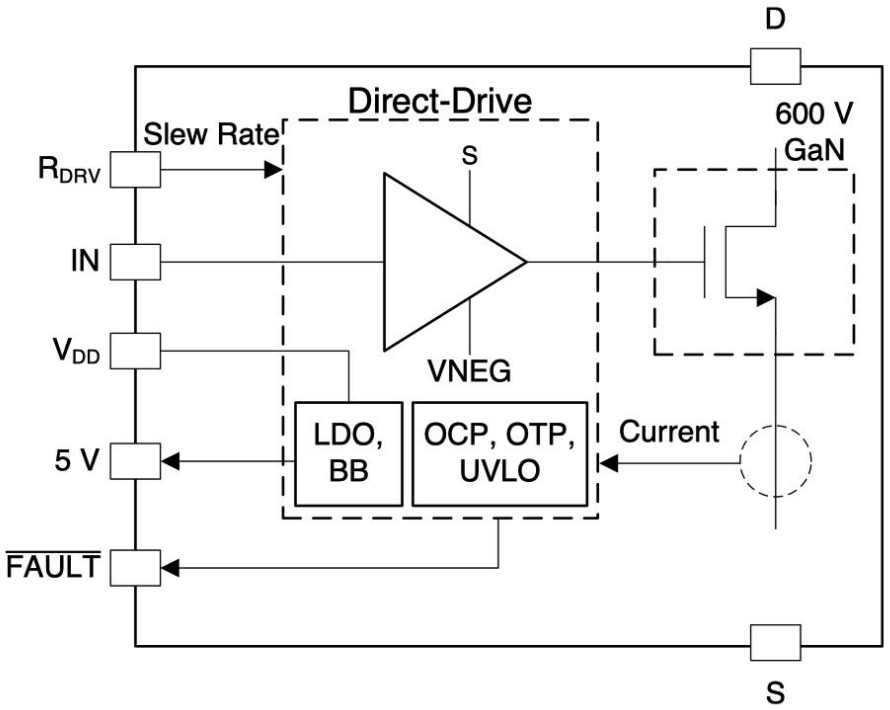
GP16501510 as HS and LS Provided by GaNPower

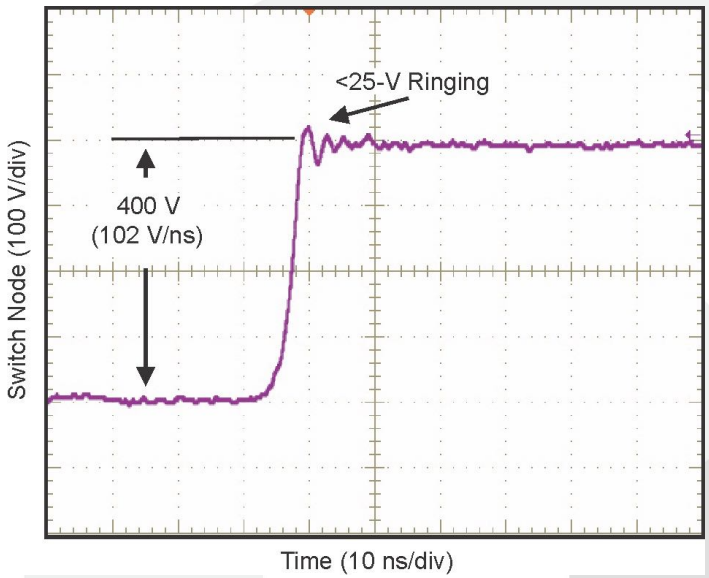


- The SenseFET from GaNPower is rated at 100V/20mΩ with two extra leads for the sensing gate and sensing source
- The current of the sensing source is designed to have a small match ratio while providing accurate sensing. However, the novelty is to use the SenseFET in a voltage clamping circuit to detect reverse conduction of the e-mode GaN low side output device while protecting the detection circuit from the high voltage swing at the switching node
- The duration of this reverse conduction is then corrected by adjusting the dead-time in the following switching cycle to ensure optimum power conversion efficiency
- The GaN SenseFET is conveniently packaged in an 8×8 8-lead DFN package

Source: W.J. Zhang, Y.H. Leng, J.S. Yu, Y.S. Lu, C.Y. Cheng and W.T. Ng, A Gate Driver IC for Enhancement Mode GaN Power Transistors with Precise Dead-time Correction, ISPSD 2019

Si Driver + GaN Co-package: TI Direct-Drive





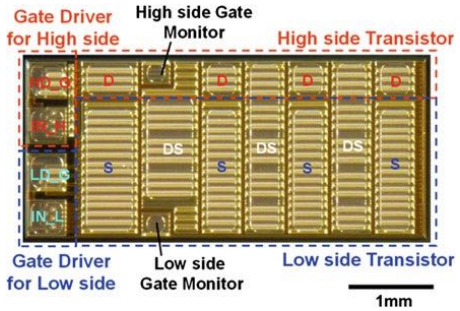
Direct-drive looks like a cascode method, in which a low voltage MOS is in series with high voltage D-mode GaN. The difference is that TI integrates the driver IC to drive the GaN directly, while the low voltage MOS is used to make the package normally-off

The voltage slew rate can exceed 100V/ns

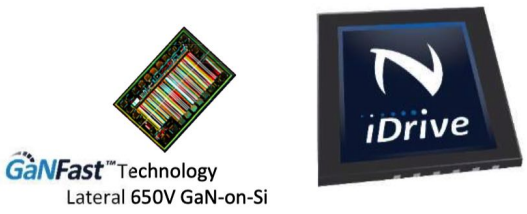
Source: LMG341xR070 600-V 70-mΩ GaN with Integrated Driver and Protection. TI datasheet

GaN IC, is it the future?

- ✓ Currently, mainstream GaN technology is using 6-inch wafer with 0.5um feature size
- ✓ This roughly equals to the silicon lateral BCD technology used 20 years ago
- ✓ GaN IC doesn't have P-type HEMT, due to ion-implantation of p-type materials such as Mg and subsequent thermal anneal very difficult to handle
- ✓ Instead, GaN IC is either using Direct-Coupled FET Logic (DCFL) with both E-mode and D-mode devices, or just use D-mode devices in the IC design
- ✓ Resistors, capacitors are available in GaN IC, much like 20 years ago in silicon BCD technology

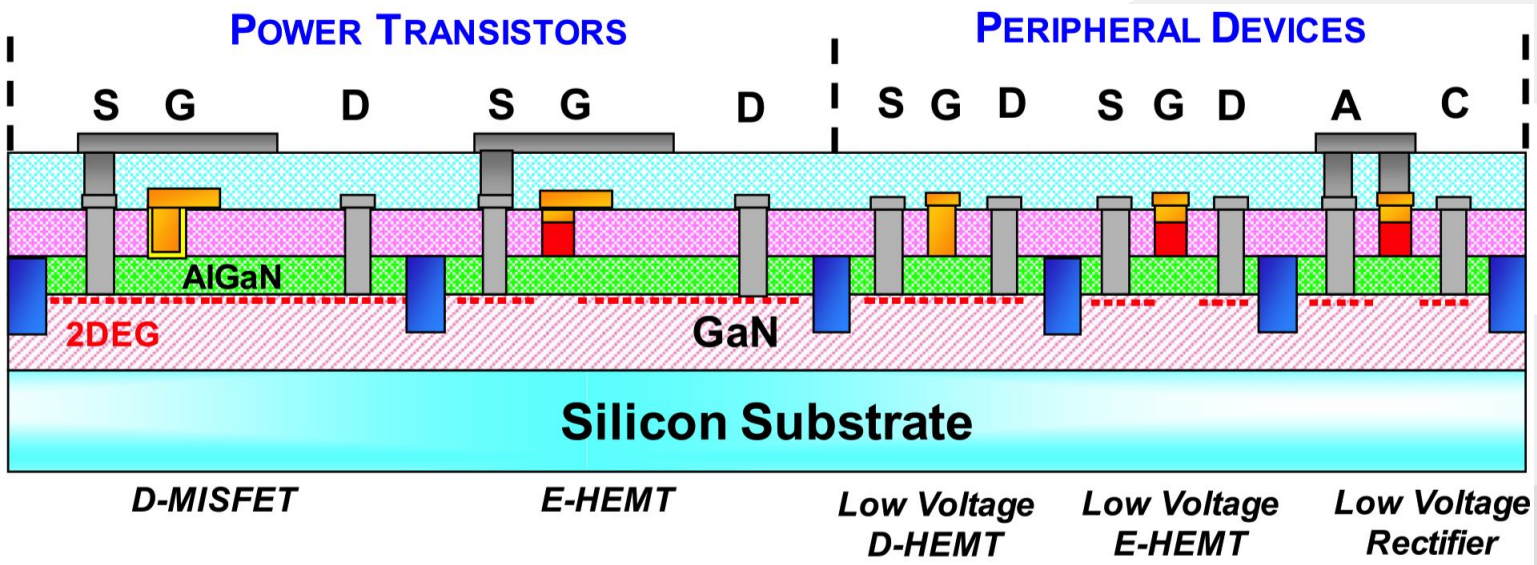


Panasonic GaN IC



- GaN-based Semiconductor Devices for Future Power Switching Systems; Hidetoshi Ishida, Ryo Kajitani, Yusuke Kinoshita, Hidekazu Umeda, Shinji Ujita, Masahiro Ogawa, Kenichiro Tanaka, Tatsuo Morita, Satoshi Tamura, Masahiro Ishida and Tetsuzo Ueda; IEDM 2016
- Navitas APEC 2019 Industry paper

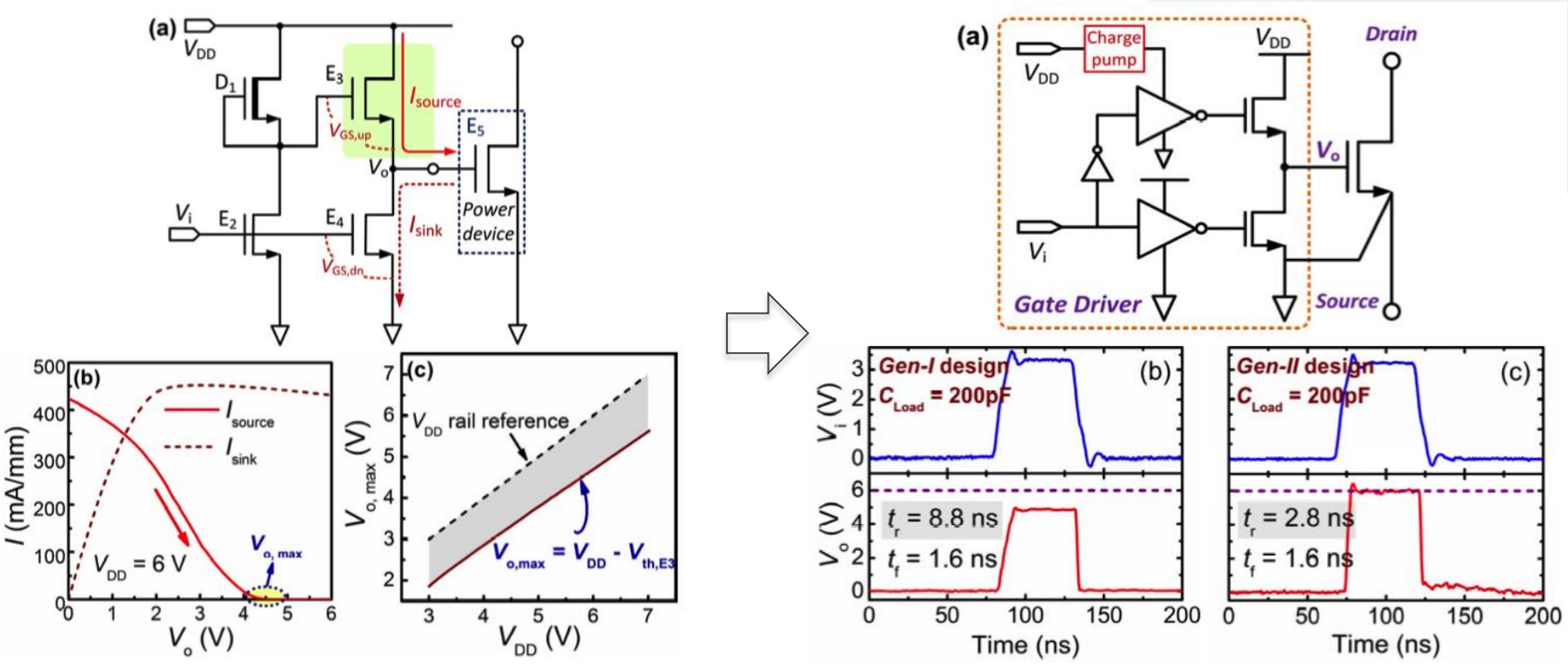
GaN IC, is it the future?



- ✓ Both active devices, such as high voltage and low voltage D-mode and E-mode HEMT are available
- ✓ Passive components, such as GaN-FET-based rectifiers, MIM capacitors and 2DEG resistors are available for analog functions

Source: Kevin J. Chen, Oliver Häberlen, Alex Lidow, Chun lin Tsai, Tetsuzo Ueda, Yasuhiro Uemoto and Yifeng Wu, GaN-on-Si Power Technology:, Devices and Applications IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017

GaN IC, is it the future?

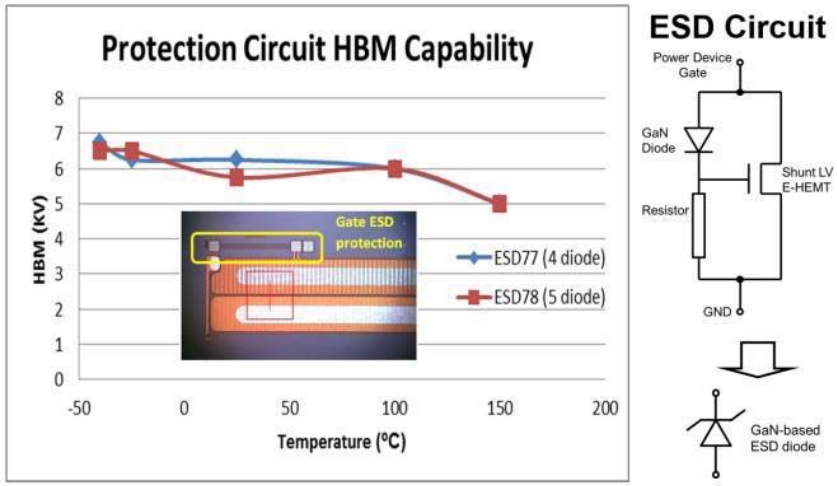


- One of the first published monolithically integrated GaN IC design with two generations using directly-coupled FET Logic that combines both D-mode and E-mode transistors

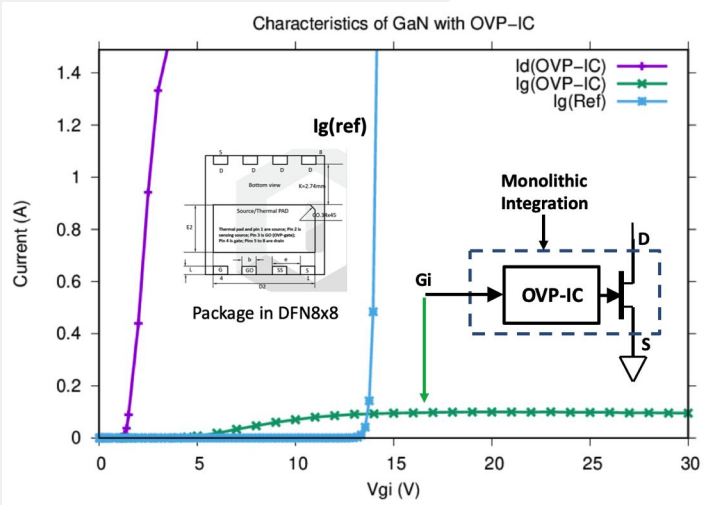
Source: Gaofei Tang1, M.-H. Kwan2, Zhaofu Zhang1, Jiabei He1, Jiacheng Lei1, R.-Y. Su2, F.-W. Yao2, Y.-M. Lin2, J.-L. Yu2, Thomas Yang2, Chan-Hong Chern2, Tom Tsai2, H. C. Tuan2, Alexander Kalnitsky2, and Kevin J. Chen1, High-Speed, High-Reliability GaN Power Device with Integrated Gate Driver; Proceedings of the 30th International Symposium on Power Semiconductor Devices & ICs May 13-17, 2018, Chicago, USA

GaN IC, is it the future?

Numerous design has been reported for GaN IC, including simple logic functions such as NAND, NOR and comparators



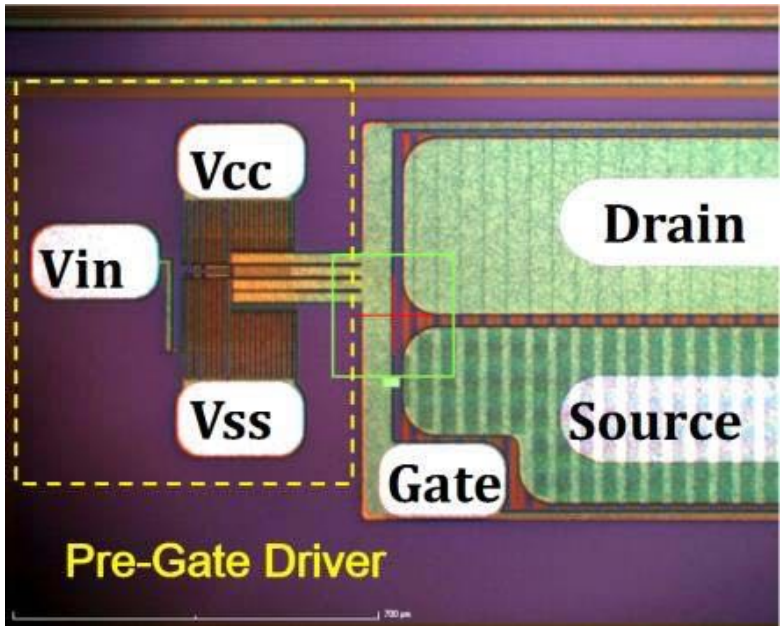
GaN integrated ESD protection circuit (<2% area) integrated to the gate of the power device on the GaN power device platform. Human body model ESD voltage on the gate can exceed 5 kV from −45 °C to 150 °C



An over-voltage-protection (OVP) function offered by GaNPower provides gate voltage protection by clamping gate voltage below required maximum gate voltage of GaN when the driver output exceed the maximum

Source: Kevin J. Chen, Oliver Häberlen, Alex Lidow, Chun lin Tsai, Tetsuzo Ueda, Yasuhiro Uemoto and Yifeng Wu, GaN-on-Si Power Technology:, Devices and Applications IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017

GaN IC, is it the future?

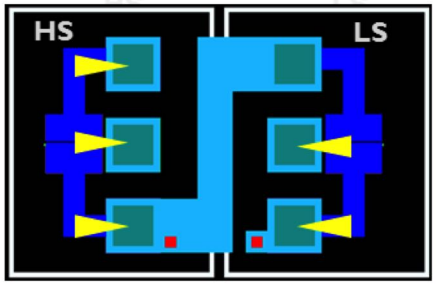


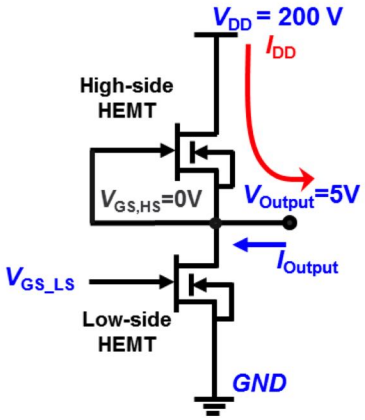
GaN integrated pre-gate driver (<5% area) integrated with a 120-mm E-mode GaN power device. Integration of devices shortens parasitic paths and thus achieves low ringing, short rise (8.5 ns) and fall (2.5 ns) time, and higher switching speed

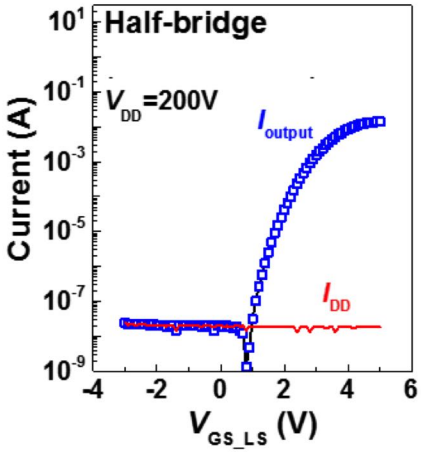
Need more detailed analysis from the application side to fully compare the benefits and drawbacks of using either monolithically integrated GaN solution or Si driver + GaN solution

Source: Kevin J. Chen, Oliver Häberlen, Alex Lidow, Chun lin Tsai, Tetsuzo Ueda, Yasuhiro Uemoto and Yifeng Wu, GaN-on-Si Power Technology:, Devices and Applications IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 3, MARCH 2017

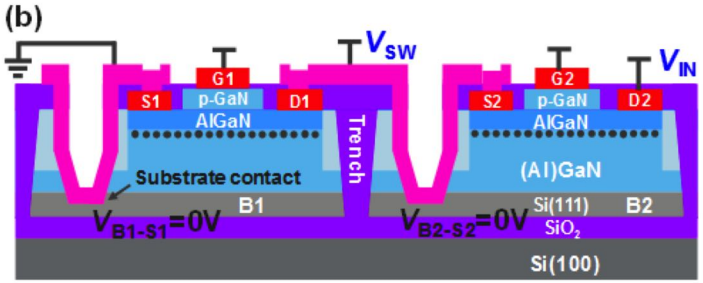
GaN IC, is it the future?

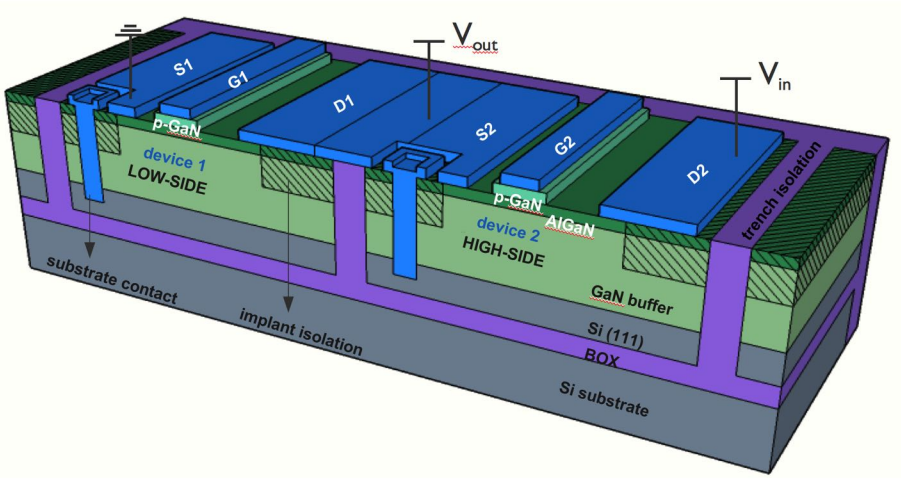






Perfect isolation between High Side and Low Side transistors in a GaN-based half-bridge on chip





Imec's GaN-IC approach

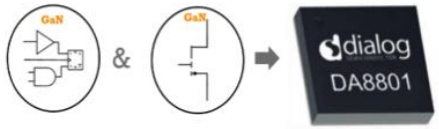
IMEC is offering GaN IC for MPW (multi-project-wafer) based on their GaN-on-SOI epitaxy.
They have also demonstrated first high-side/low-side GaN-IC on chip with perfect isolation

Source: https://www.imec-int.com/en/200mm-GaN-on-Si-technology

GaN IC, is it the future?

GANPOWER INTERNATIONAL

dialog SEMICONDUCTOR

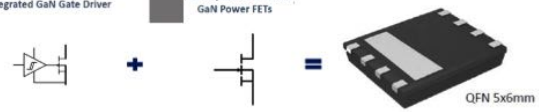


Monolithic solution

Navitas

First & Fastest integrated GaN Gate Driver

Fastest, most efficient GaN Power FETs



Power devices integrated with drivers and other analog IC functions

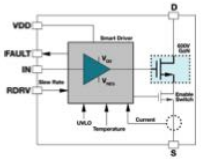
Power devices integrated with drivers in the same chip

System-in-package solution

GANPOWER INTERNATIONAL

TEXAS INSTRUMENTS

Power devices and driver IC chips in the same package

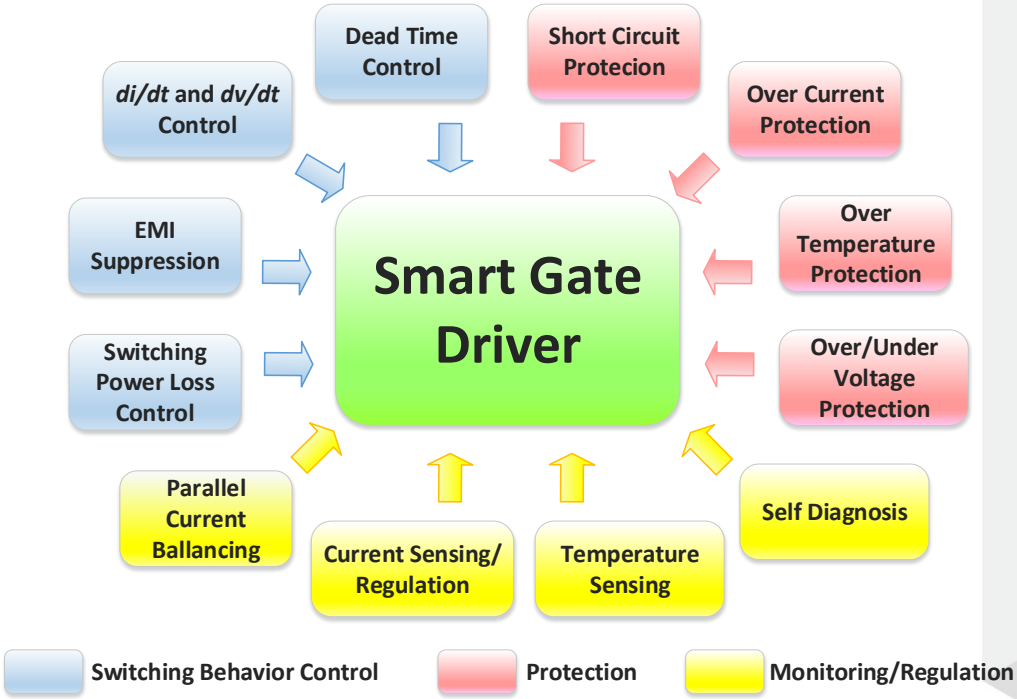


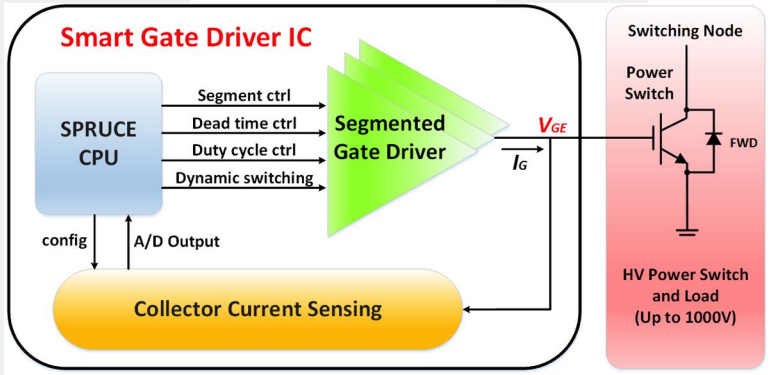
Discrete

(From Yole Development with modifications). Gate Drivers market evolution: coreless isolation and WBG specific solutions, Yole Development, APEC 2018

GaN IC, is it the future?

While monolithic integration provides ultimate performance and eliminates on-board parasitics, silicon IC + GaN co-package can still provide more comprehensive functionalities -- at least for now





Ref: Design Trends in Smart Gate Driver ICs for Power MOSFETs and IGBTs, ASICON 2017

GaNPower Future Integrated Modules

GaNPOWER
Integrated Power Module

THANKS FOR WATCHING!

Contact us （Vancouver Headquarters）:

230-3410 LOUGHEED HWY VANCOUVER, BC, V5M 2A4 CANADALGA

1.778.588.1119

information@iganpower.com

联系我们 (Greater China Region)

中国江苏省苏州市工业园区纳米技术国家大学科技园F0411

+86-512-65267027

sales@iganpower.com

GaNPOWER

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WWW.IGANPOWER.COM

230-3410 LOUGHEED HWY

VANCOUVER, BC, V5M 2A4 CANADA