GaNPower International Inc.

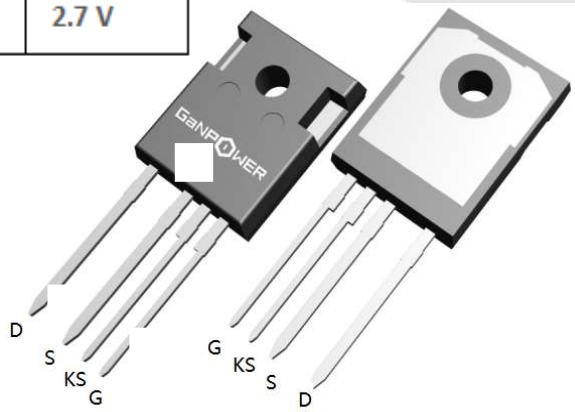
GP120R60T4

N-channel 1100V 30A GaN Power HEMT in TO247-4 Package

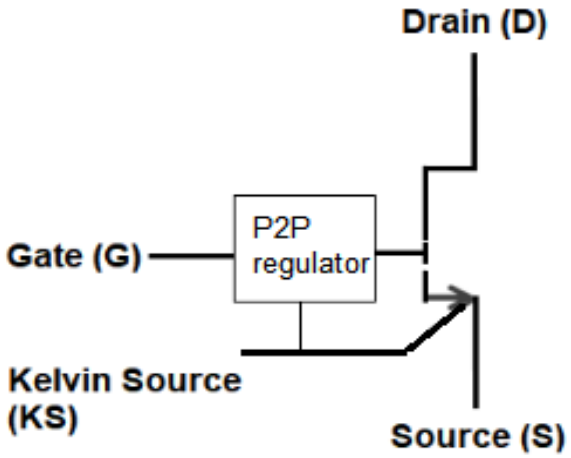
Datasheet version 1.0 Preliminary

Features

BV_{dss}	R_{dson}	I_{ds}	Q_g	V_{GS}	Vgs(TH)
1100 V	60 mO	30 A	8.25 nC	-20 to 20V	2.7 V



- Ultra-low RDS(on)
- High dv/dt capability
- Extremely low input capacitance
- Zero Qrr
- Outstanding switching performance
- Low Profile
- **Upgrated P2P-GaN with input regulator IC to to match input lead and voltage of existing SiC MOSFET**



Applications

- Switching Power Applications
- Server and Telecom Power Application
- EV OBC and DC-DC Converters
  UPS, Inverters, PV

Description

These devices are N-channel 1100 V Power GaN HEMTs based on proprietary E-mode GaN on silicon technology, integrating an input regulator circuit to match input lead and voltage of existing SIC MOSFET in a pin to pin fashion. The resulting product has extremely low on state resistance, very low input capacitance and zero reverse recovery charge making it especially suitable for applications which require superior power density, ultra-high switching frequency and outstanding efficiency.

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Device Characteristics

Static Parameters				Test data			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$V_{gs(TH)}$	Gate threshold voltage	$V_{ds}=V_{gs}$, I_d=21 mA (T_J=25 °C)	1.5	2.7	4	V
2	V_{GS}[1]	Gate-Source voltage range		-20		20	V
3	BV_{dss}[2]	Drain-Source breakdown voltage	V_{gs}=0V, I_d < 1 mA (T_J=25 °C)		1100		V
4	I_{dss}	Zero gate voltage drain leakage current	V_{gs}=0V,V_{ds}=1100V T_J=25°C		250	950	μA
5	I_{gss}	Gate-Source Leakage	V_{gs} = 6V, V_{ds} = 0V		0.7	30	mA
6	R_{dson}	drain-source on resistance	V_{gs}=6.5V, I_d=6A T_J=25°C		42	60	mΩ
7	V_{sd}	Reverse conduction voltage	I_{sd}=0.5A, V_{gs}=0V	1.2	2.0	3	V
8	R_g	Gate resistance	f=25Mhz Open drain		1.5		Ω

Dynamic Parameters				Test data			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	C_{ISS}	Input capacitance	V_{gs} = 0 V V_{ds} = 700 V f = 1MHz		236		pf
2	C_{OSS}	Output capacitance			72		pf
3	C_{RSS}	Reverse transfer capacitance			4.6		pf
4	Q_g	Gate charge	Vds = 400V Id = 9A Vgs = 6V		8.25		nC
5	Q_{gs}	Gate to source charge			1.5		nC
6	Q_{gd}	Gate to drain charge			1.8		nC
7	Q_{rr}	Reverse recovery charge			0		nC

Switching Performance				Test data			
	Parameters		**Conditions**	**Min**	**Typical**	**Max**	**Unit**
1	$t_{d(on)}$	Turn-on delay time	V_{ds} = 800V I_d = 15A		34		ns
2	t_r	Rise time			26		ns

[1] A wider range of gate driving from-20V to 20V can be accepted, but recommended range is still -3V to 6V. Wider range protects the gate from damage, but at some cost of power loss.

[2] BV_{dss} refers to DC withstanding voltage. This product is recommended for DC bus voltage of 800-1000V.

3	$t_{d(off)}$	Turn-off delay time	R_g = 10Ω V_{gs} = -3/6.5V		33		ns
4	t_f	Fall time			20		ns

Absolute Max. Ratings

	Symbols	Parameters	Value	Unit
1	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=25 °C	1100	V
2	$V_{DS\text{-}max}$	Breakdown voltage transient @ T_{case}=125 °C	1000	V
3	$V_{GS\text{-}max}$	Gate to source max. voltage @ T_{case}=25°C	-12 to +7.5	V
4	$I_{ds\text{-}max}$	Drain to source pulse current @ T_{case}=25 °C, pulse width 10 µs, V_{GS} = 6 V	30	A
5	$I_{ds\text{-}max}$	Drain to source pulse current @ T_{case}=150 °C	22	A
6	$dv/dt_{\text{-}max}$	Drain to source voltage slew rate	200	V/ns
7	$T_{J\text{-}max}$	Max junction temperature	150	°C
8	$T_{S\text{-}storage}$	Storage temperature	-55 to 150	°C

Thermal and Soldering Characteristics (Typical)

	Symbols	Parameters	Value	Unit
1	R_{thJC}	Thermal resistance (junction to case)	0.6	°C /W
2	R_{thJA}	Thermal resistance (junction to ambient)	62	°C /W
3	T_{solder}	Reflow soldering temperature	250	°C

Ordering

Order Code	Package Type	Packaging Method	Qty
GP120R60T4	TO274-4 surface mount, bottom cooled	3	

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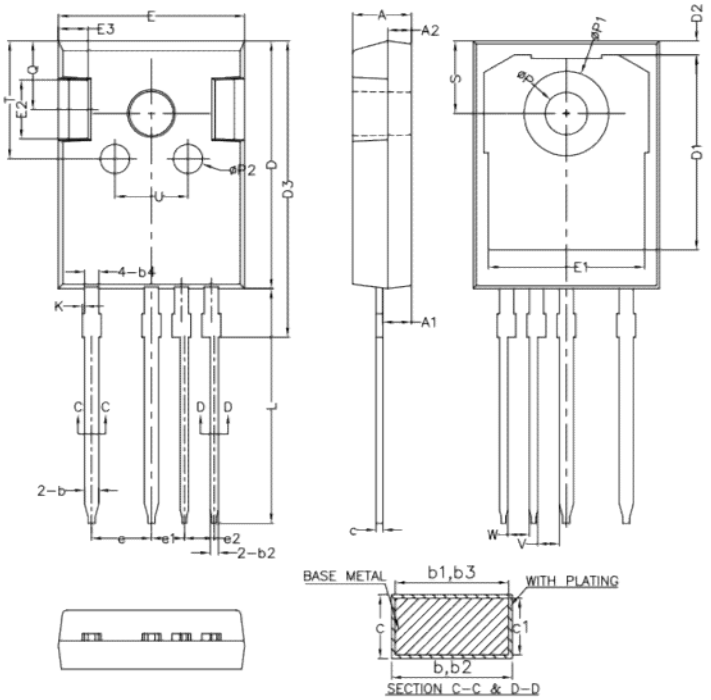
Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16	–	1.29
b1	1.15	1.20	1.25
b2	0.66	–	0.79
b3	0.65	0.70	0.75
b4	1.16	–	1.29
c	0.59	–	0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	4.98	5.08	5.18
e1	2.69	2.79	2.89
e2	2.44	2.54	2.64
K	0	–	0.20
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1	–	–	7.40
P2	2.40	2.50	2.60
Q	5.60	–	6.00
S	6.00	6.15	6.30
T	9.80	–	10.20
U	6.00	–	6.40
V	1.44	1.84	2.24
W	1.44	1.84	2.24

NOTES:
1.ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2.EJECTION MARK DEPTH $0.10^{+0.15}_{-0.05}$.

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Further information

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Data Source– Data here are based on recent tests but all parameters may not be up to date. Actual final test data from packaging production are available for selected customers upon request.